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ATLAS activity in KU

Shohei Shirabe

Kyushu University

21.02.2024

LHC and ATLAS

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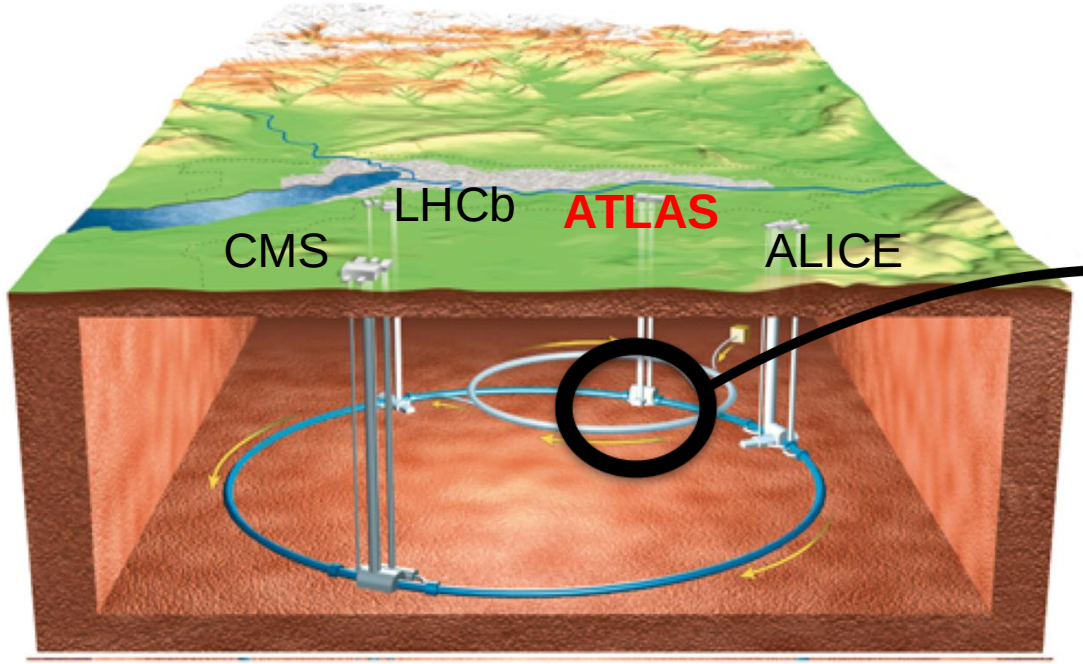
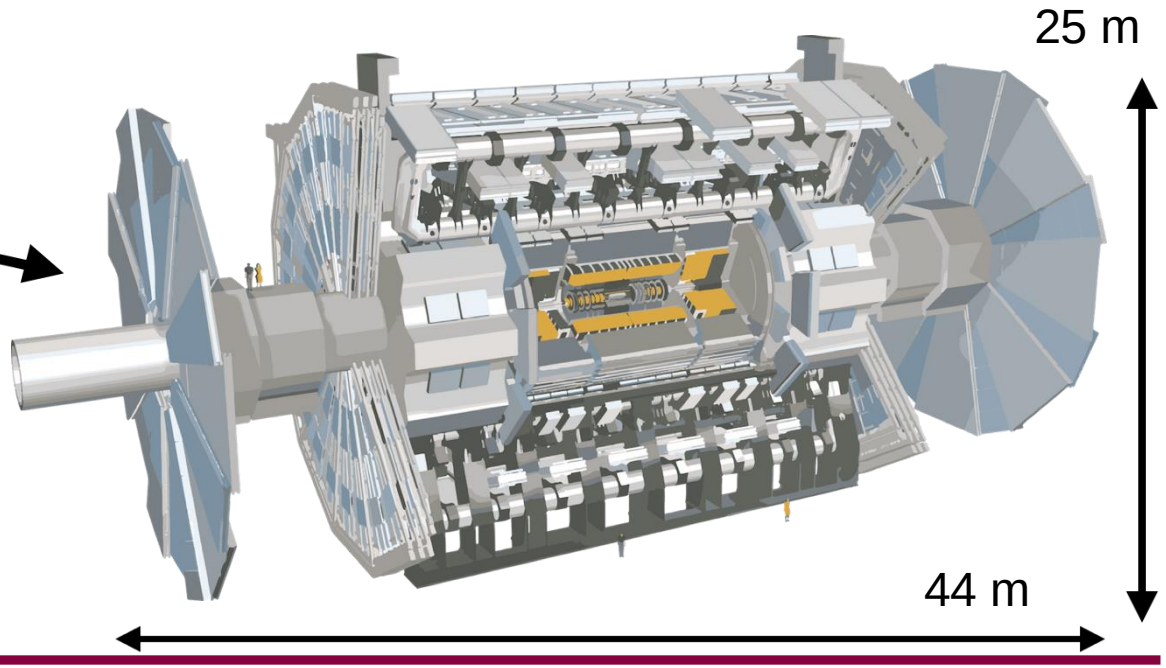
LHC

- Run3 (2022 - 2026)
- $\langle\mu\rangle \sim 60$
- $2.3 \times 10^{34}\ cm^{-2}s^{-1}$
- 300 fb^{-1} (183 fb^{-1} so far)





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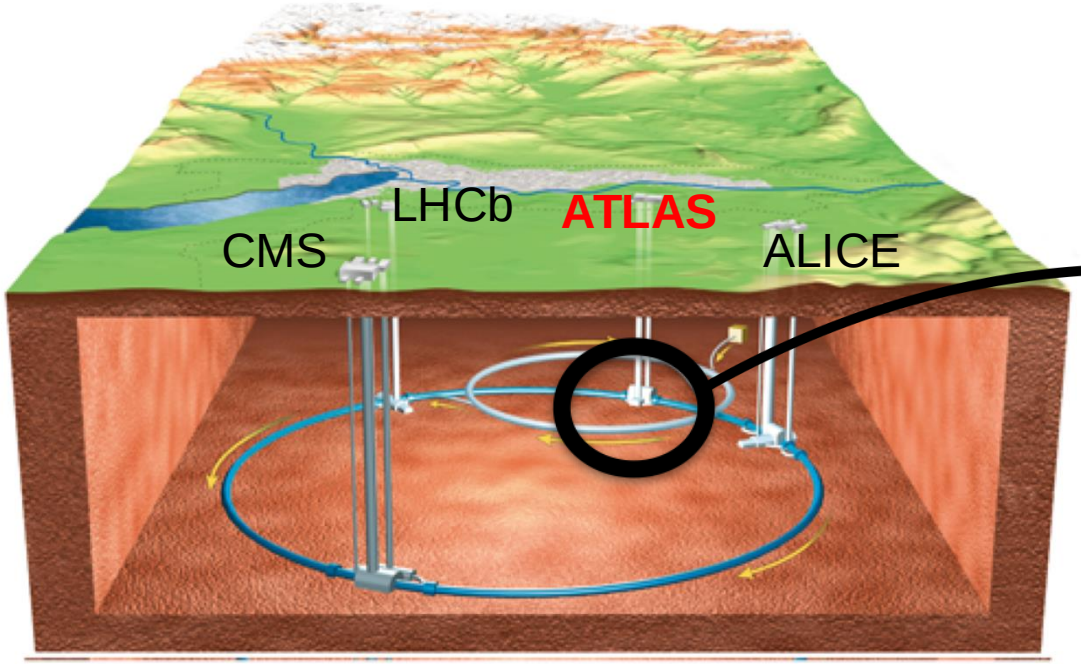
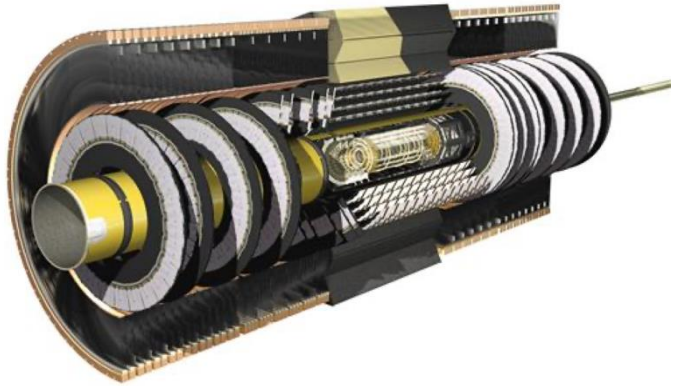
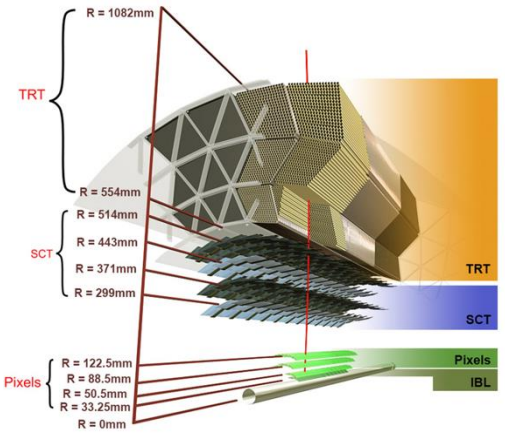
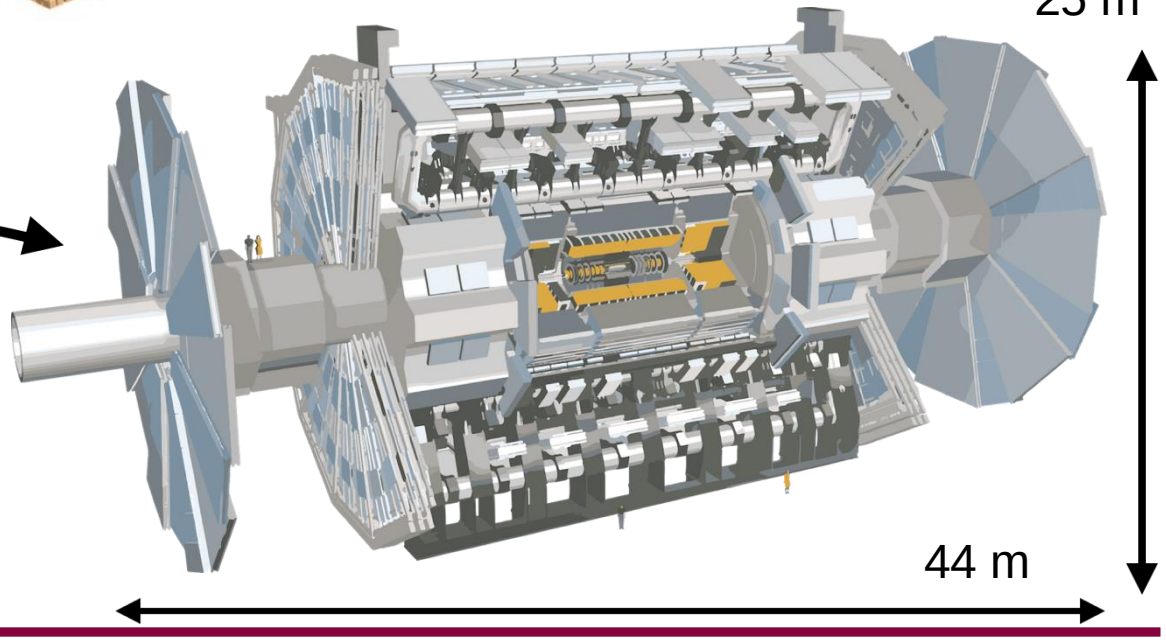


ATLAS "Current" Inner Detector







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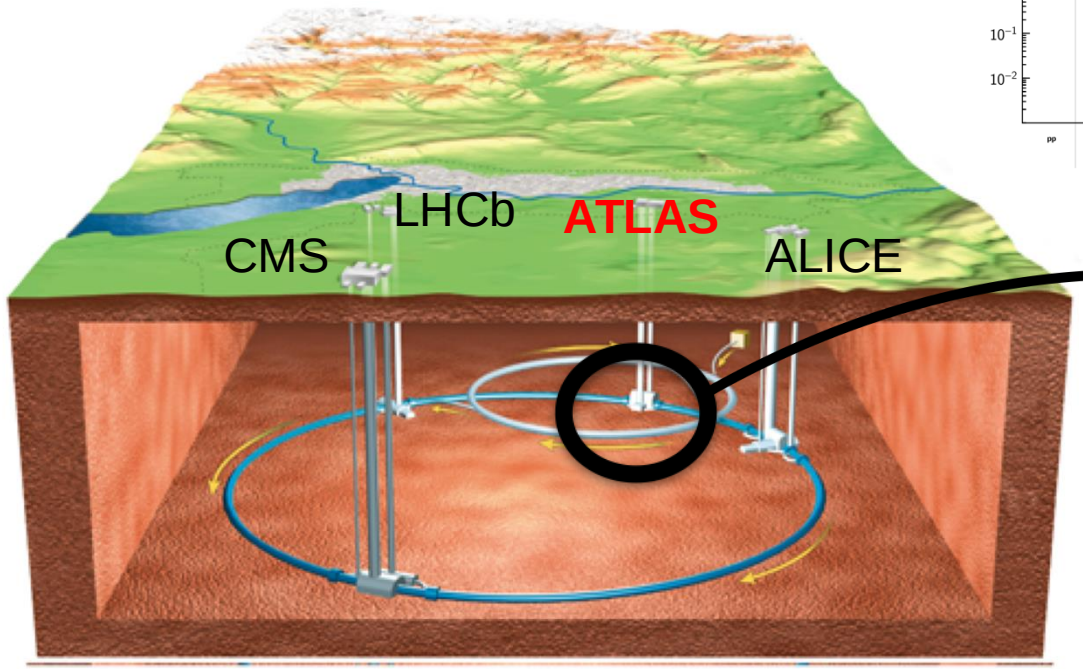

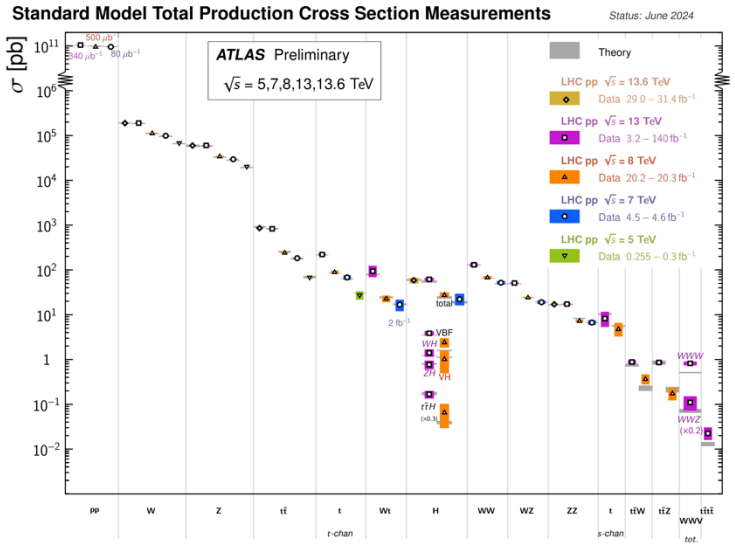

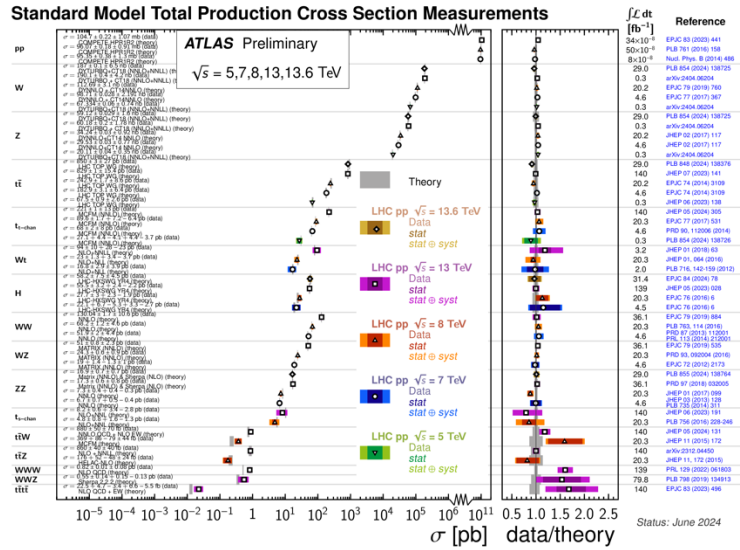

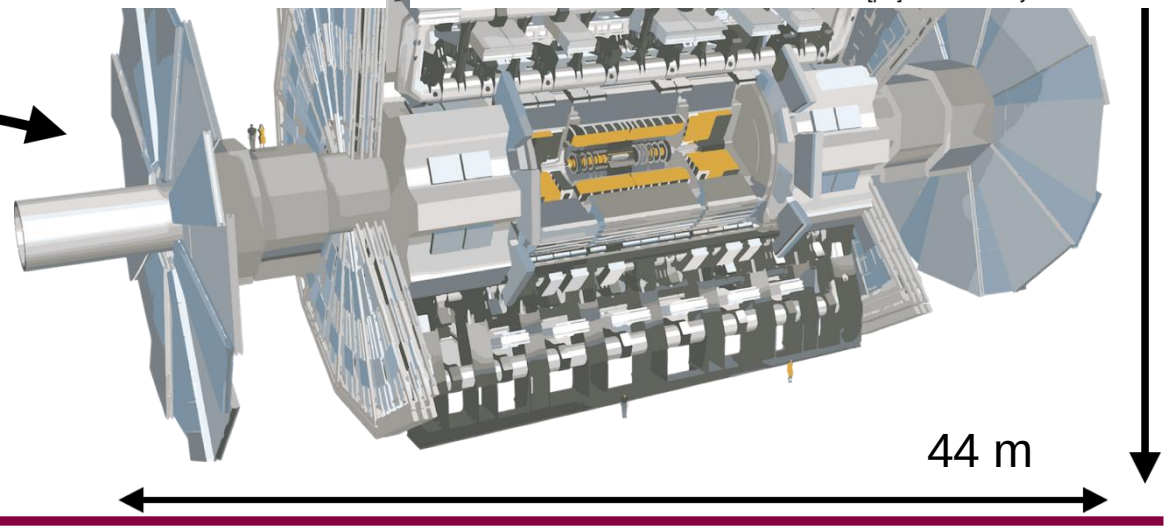

HL-LHC Upgrade

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LHC

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- 2.3 x 10^{34} $cm^{-2}s^{-1}$
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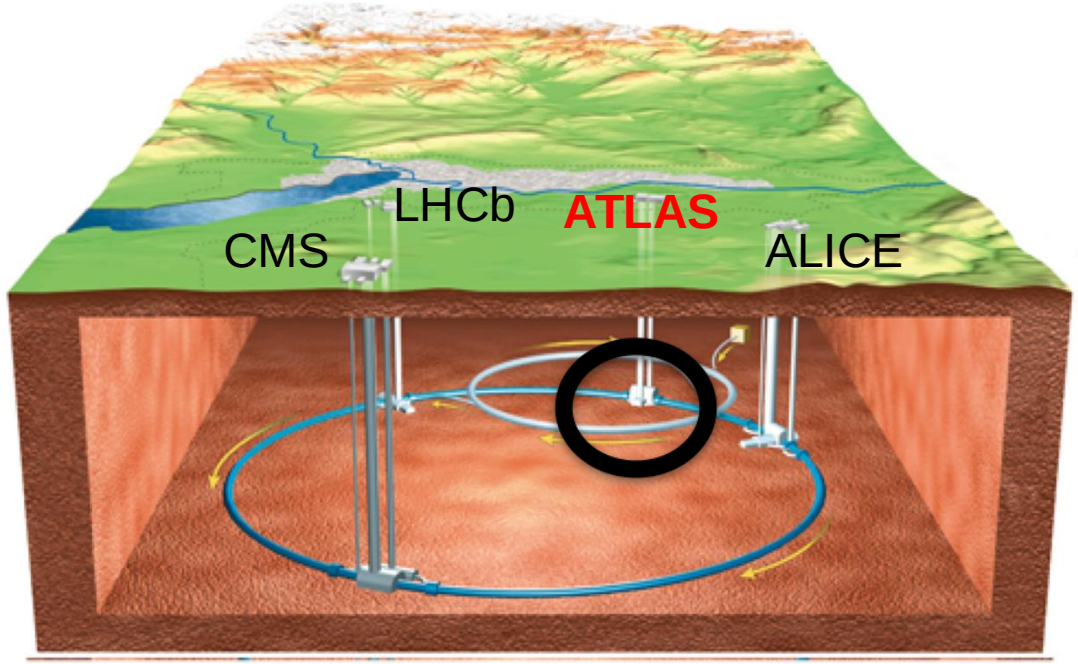
HL-LHC

- 2030 -
- <μ> ~ 60
- 5.0 (7.5) x 10^{34} $cm^{-2}s^{-1}$
- 3000 fb^{-1} (183 fb^{-1} so far)



Physics Motivation

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LHC

- Run3 (2022 - 2026)
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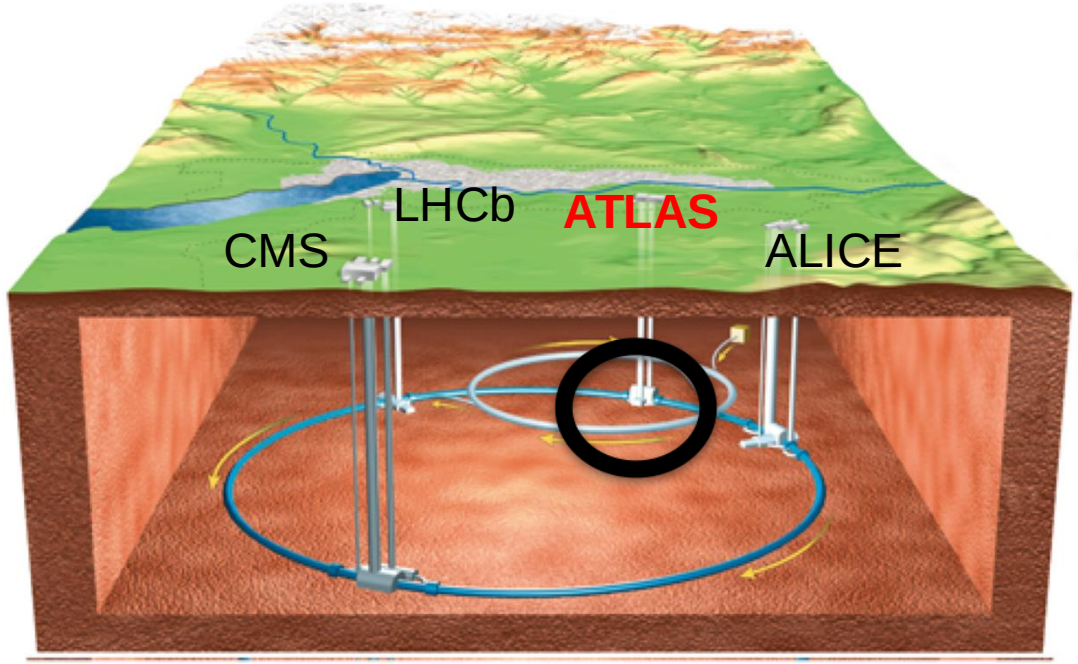

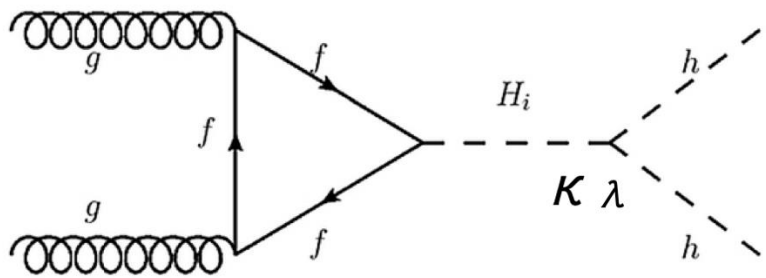

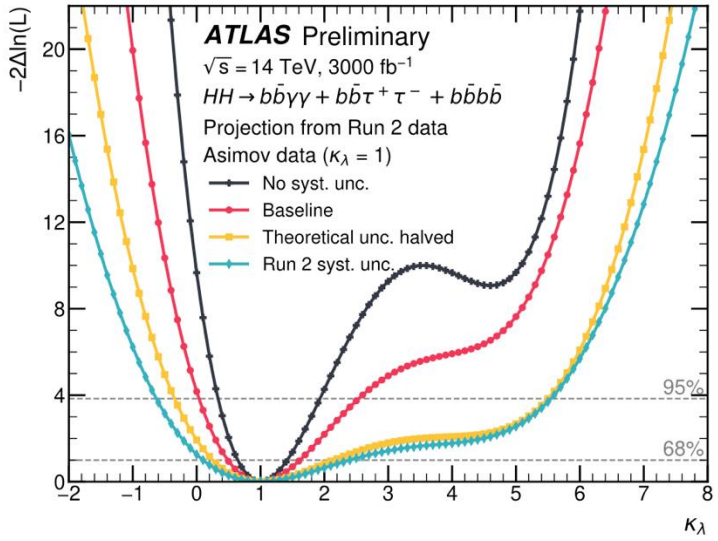

ITk Upgrade

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LHC

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HL-LHC

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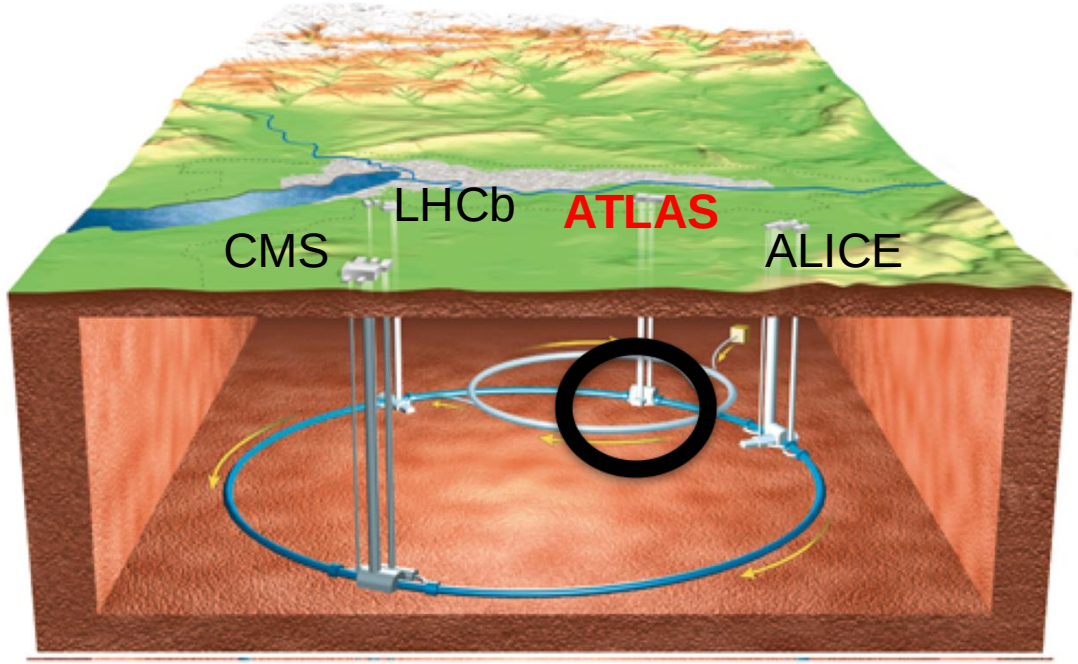

Requirement for the pixel detector and its readout becomes demanding

- **Radiation tolerance**
  - Current ID Pixel designed for ~ 400 fb^{-1}
- **Bandwidth saturation**
  - Current ID designed to accommodate $<\mu>$ ~ 50 at 2 x 10^{34} cm^{-2} s^{-1}

ITk Upgrade

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LHC

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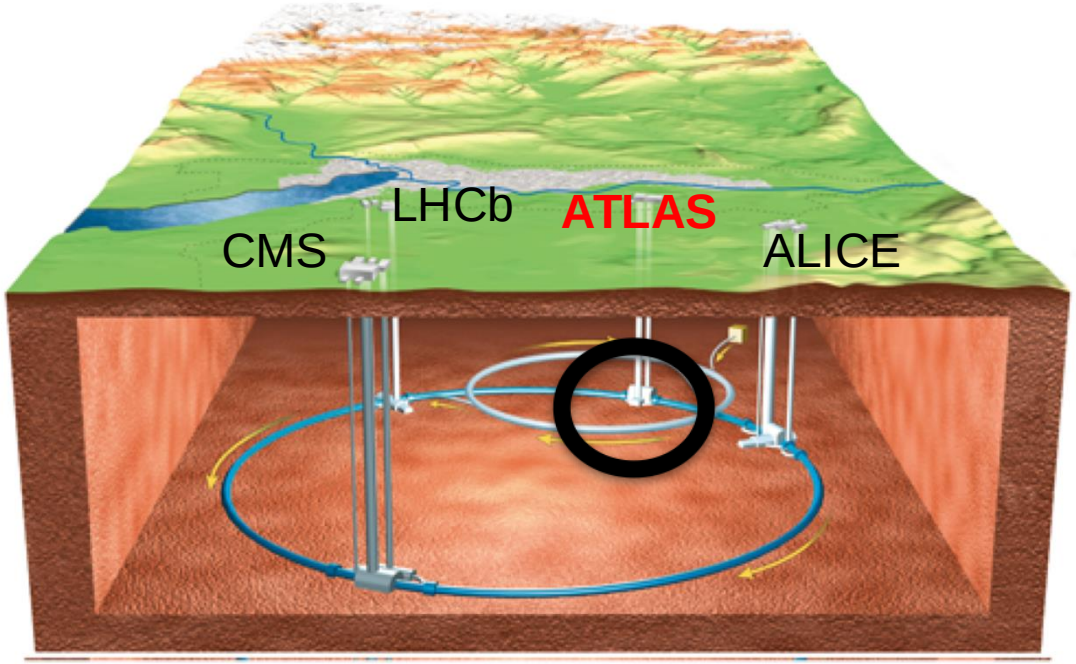
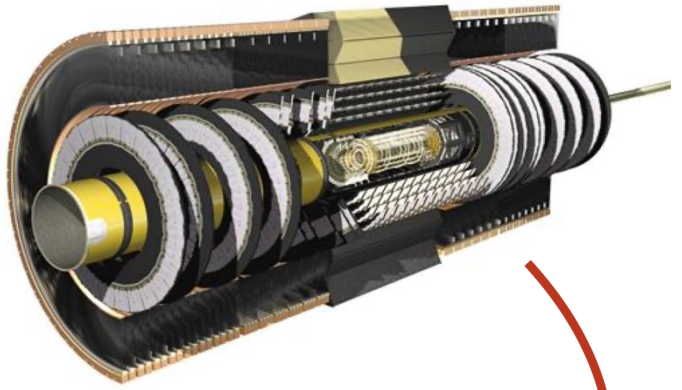
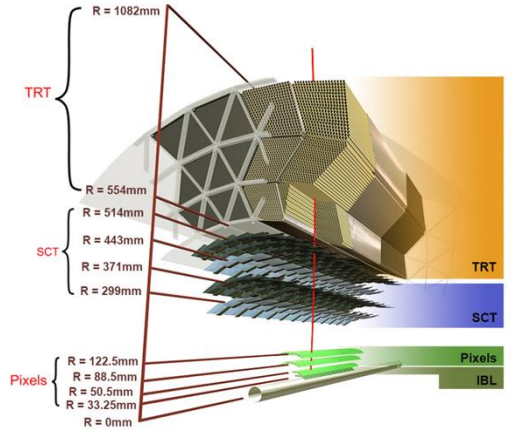
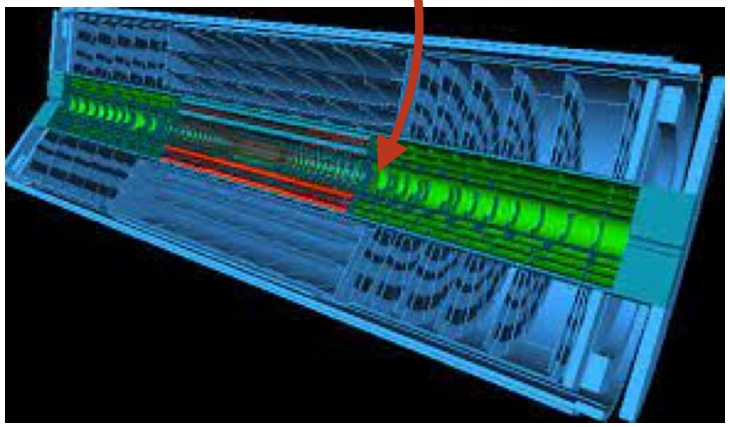


ATLAS "Current" Inner Detector







The current Inner Detector will be replaced by an all silicon Inner Tracker

ITk Layout

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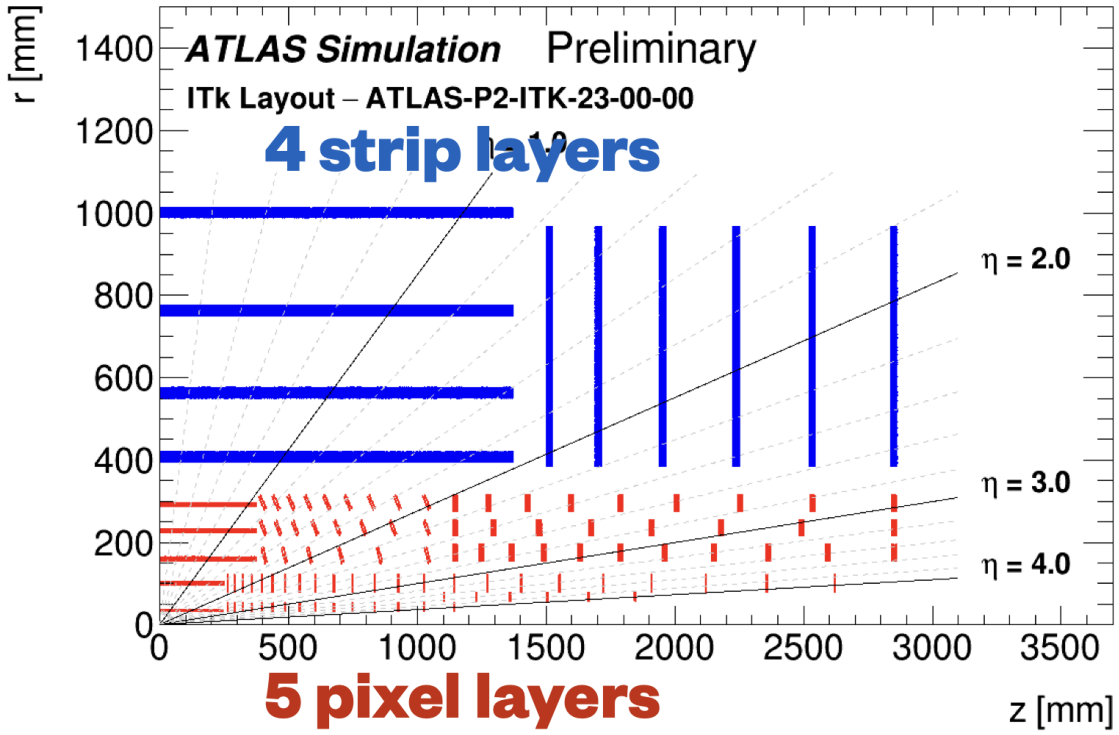
- **New Inner detector must cope with the HL-LHC environment**
  - **Better radiation tolerance**
    - Fluence of 2 x 10^{16} n_{eq}/cm^2, 4000 fb^{-1}
  - **Faster readout**
    - 5 Gbit/s per data link
  - **Finer granularity**
    - keep ~ 1% occupancy



ITk Key Concepts

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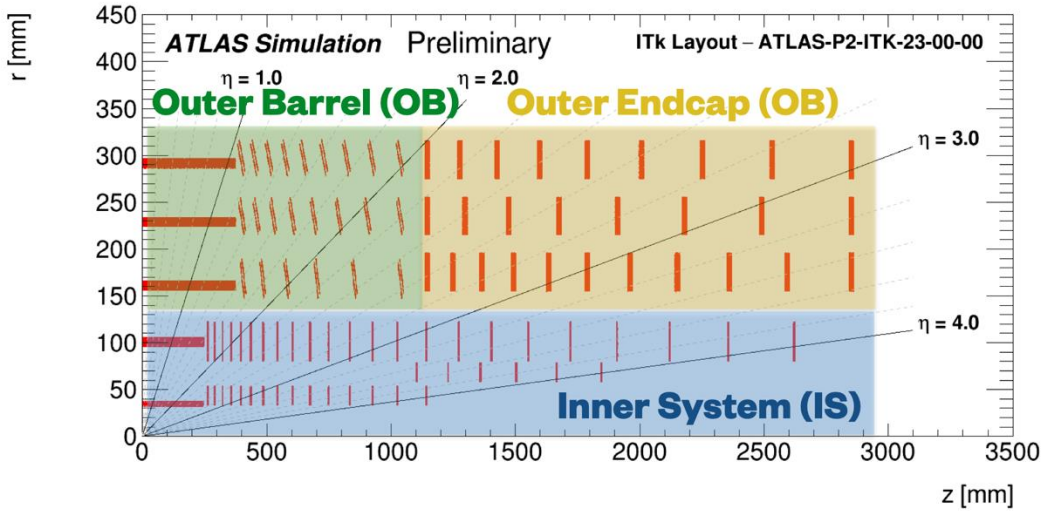
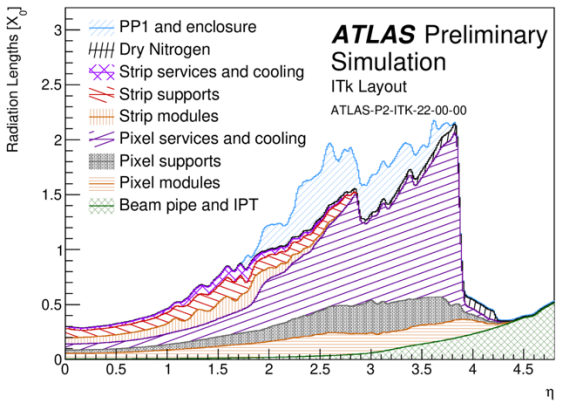
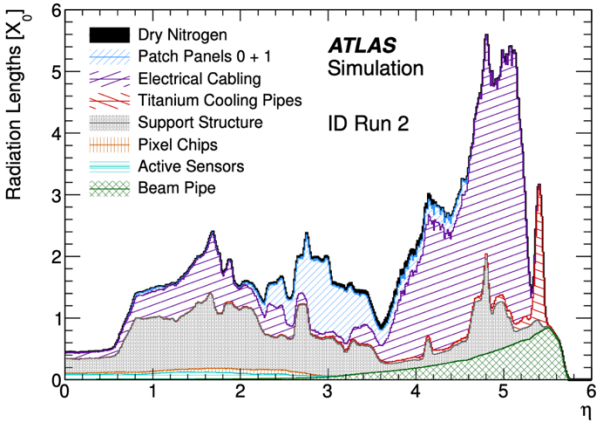
- Inner 2 layers are replaceable
- Inclined modules
  - Minimise material and maximise acceptance
- Larger covered area: 13 m^2, $|\eta| < 4$
  - Consists of ~ 10000 modules
- Low material budget
- Serial powering
- Common front-end chip for all layers
- 3D and planar sensors



Radiation length





ITk Production Flow

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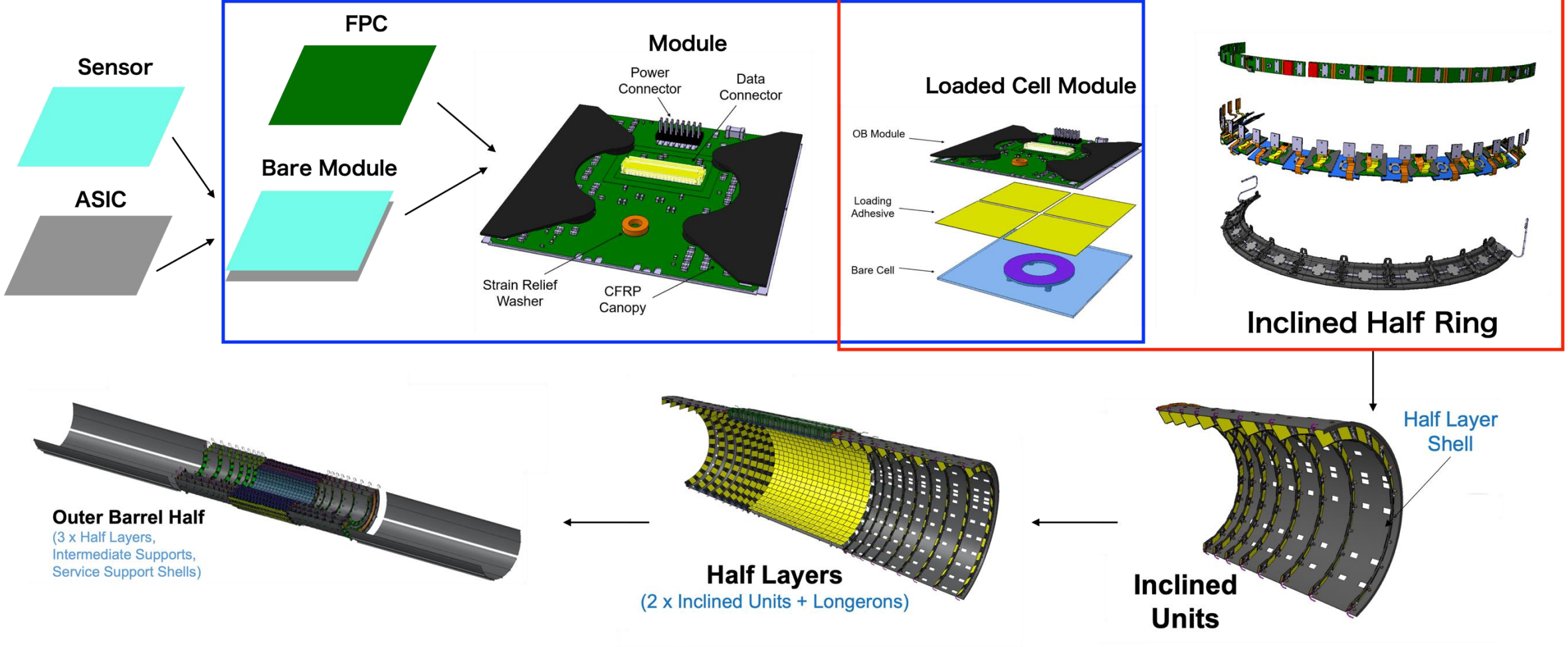
Module Assembly

Cell Loading/Integration



ITk Pixel Module

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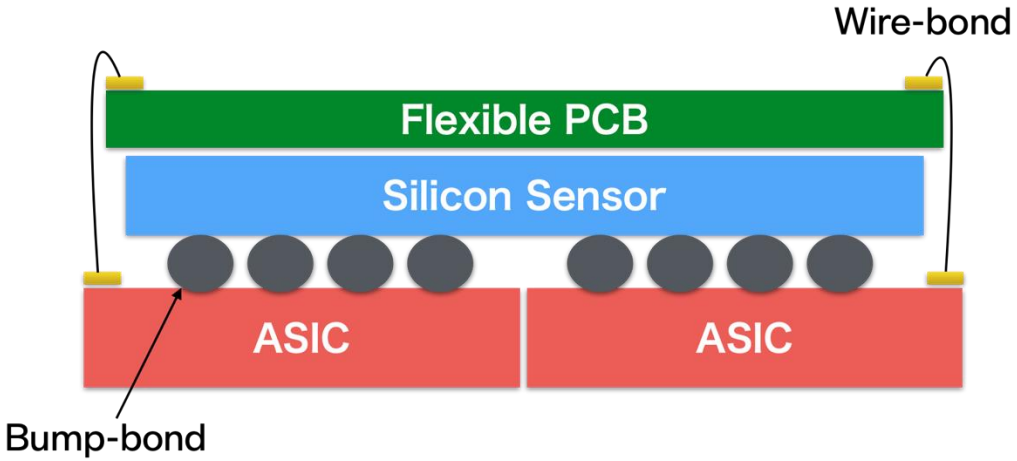
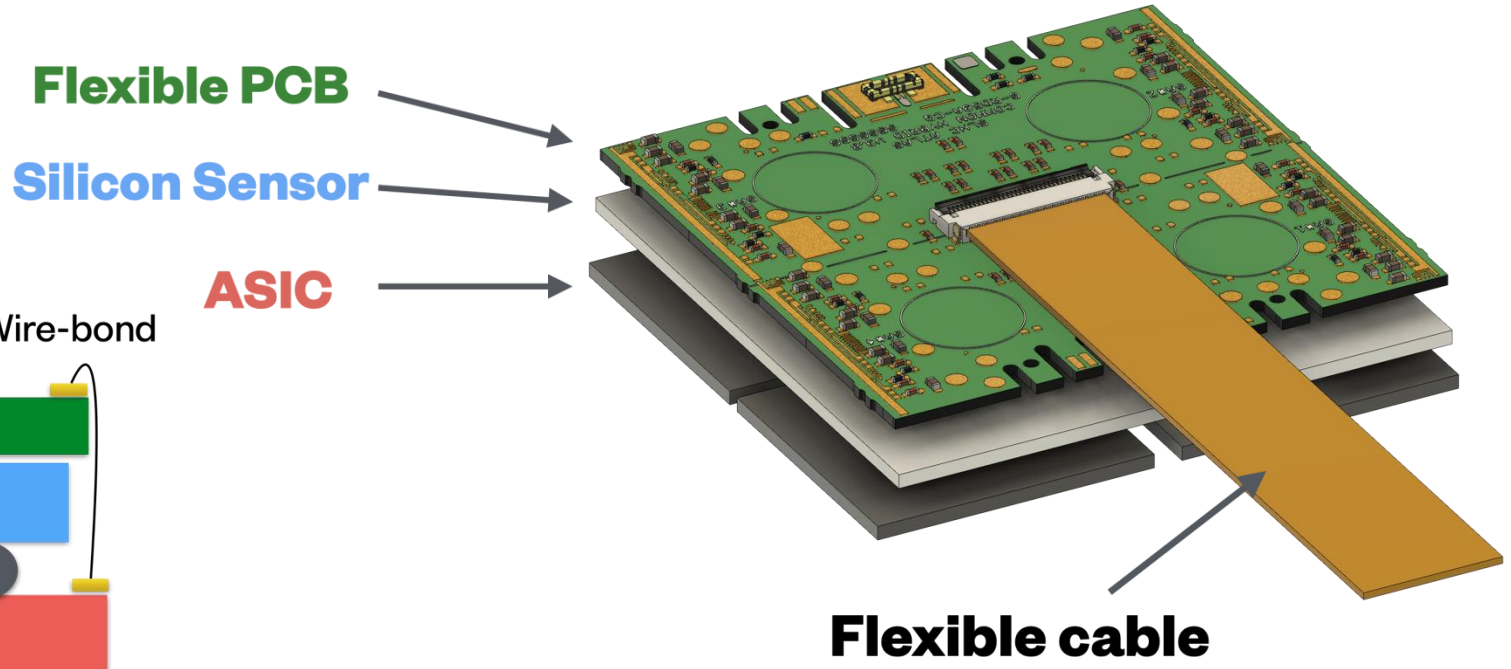
Hybridization

- Fine-pitch bump-bonding
- Bump deposition, UBM, flip chip



Quad module (40 x 40 mm2)



50 x 50 μm^2 pixel
1.28 Gb/s per lane

2,200 (+ 600) modules (1/4 of total amounts) produced in Japan

ITk Activity in Japan

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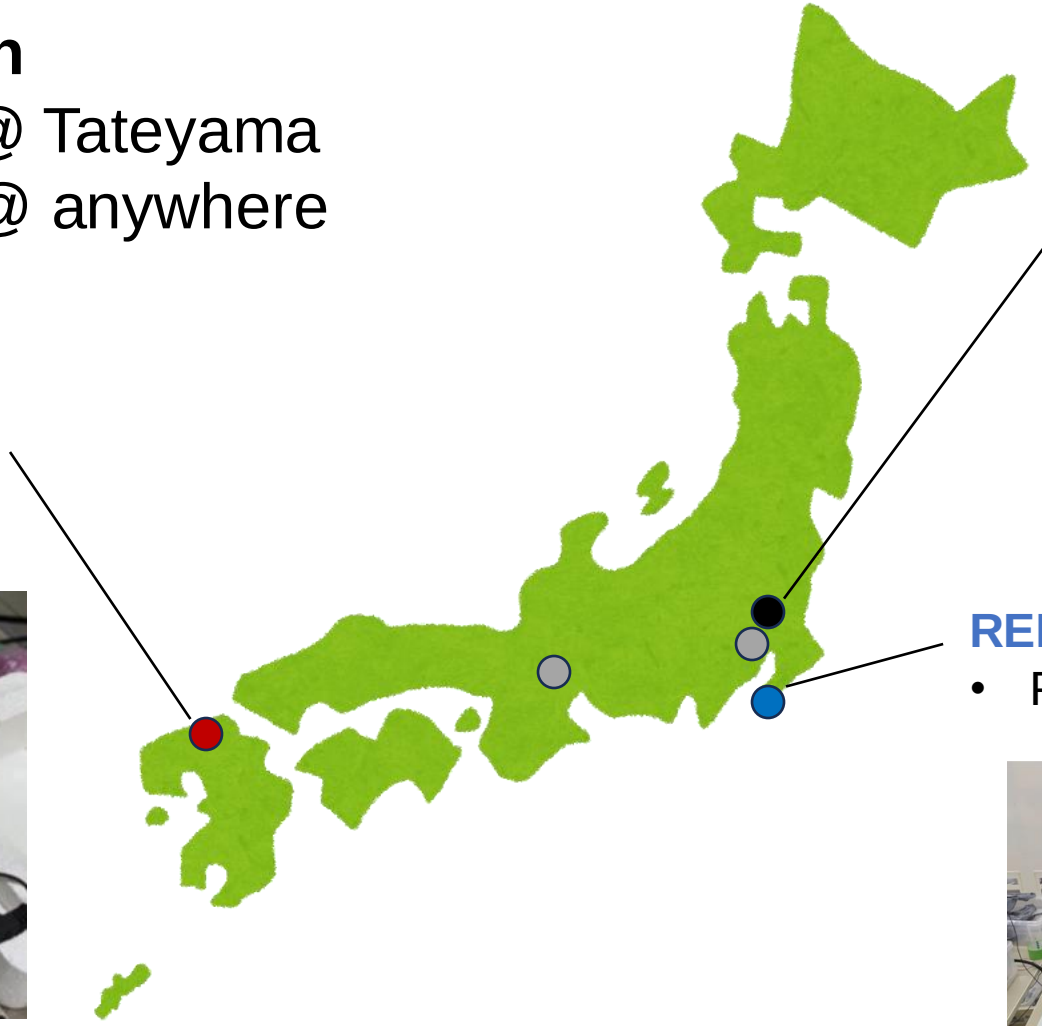
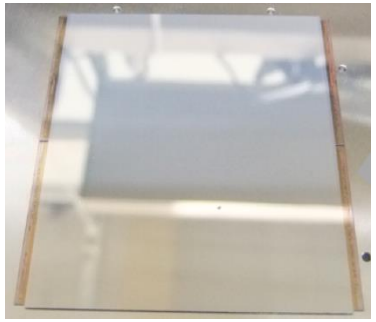
Module Production

- 3 on-site shifter @ Tateyama
- 5 remote shifter @ anywhere



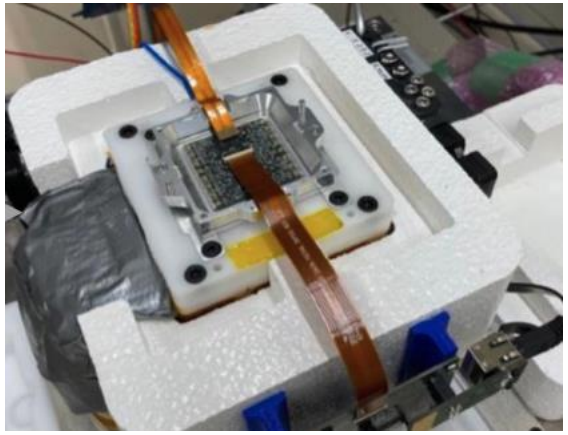
KEK @ Tsukuba

- testing site of bare-modules



KU @ Fukuoka

- satellite site
- developing the system



REPIC @ Tateyama

- Production and testing site of modules

Module Testing

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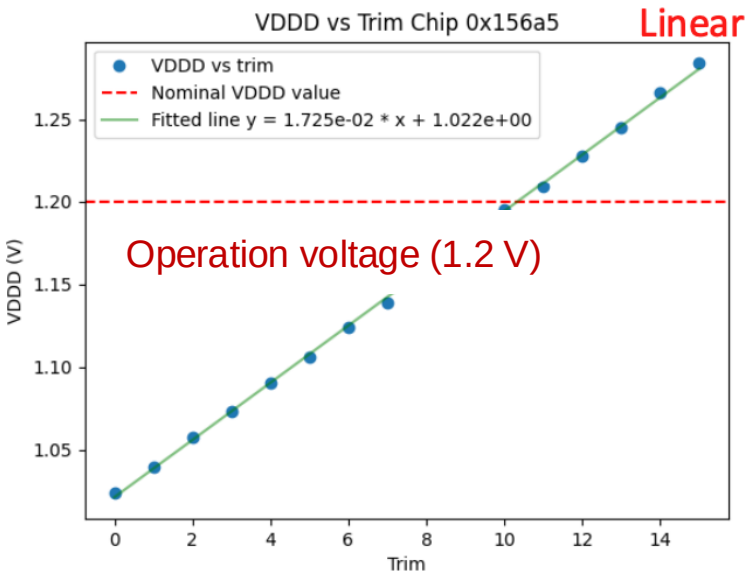
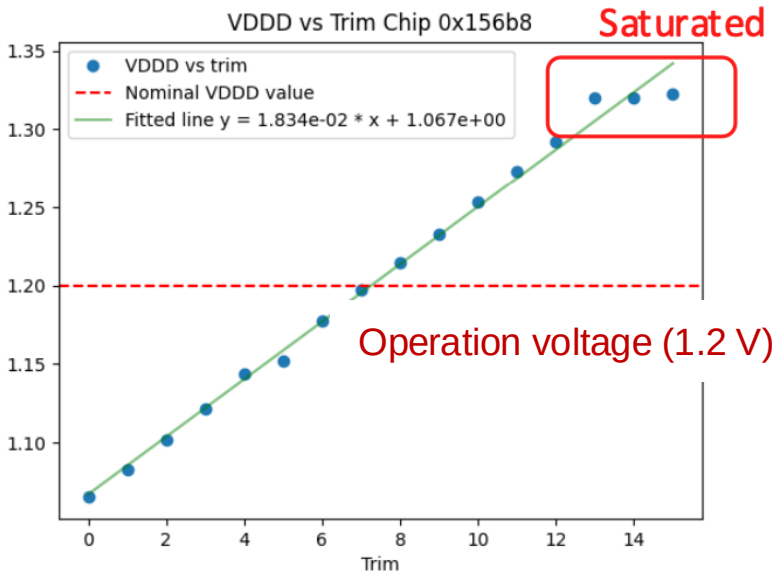
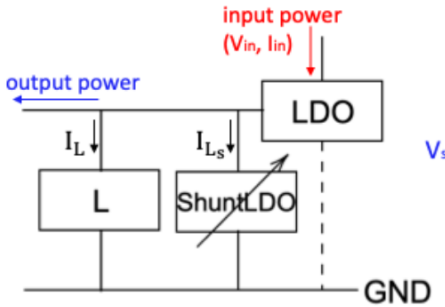
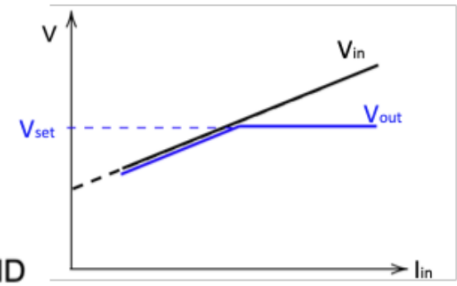
- “Pre”-Production
  - 140 modules have been produced in Japan
  - demonstrate and evaluate production and testing procedure









Cell Loading / Integration

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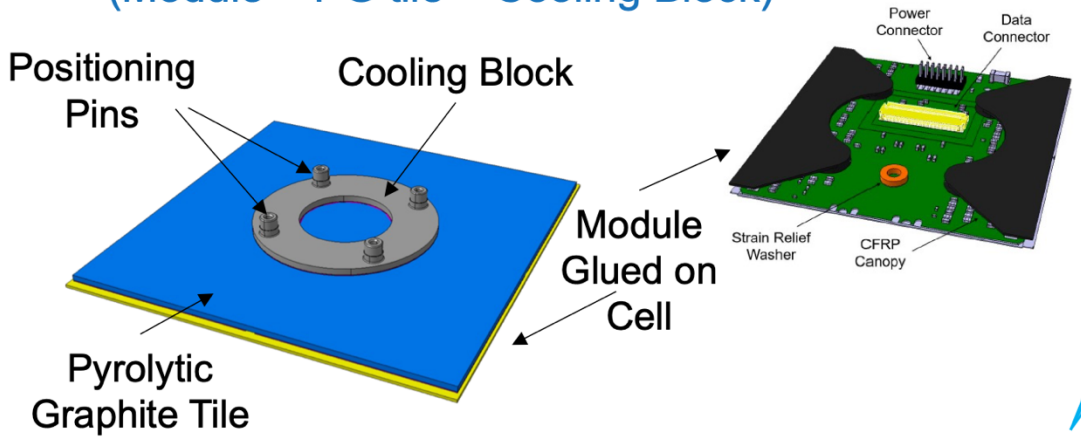
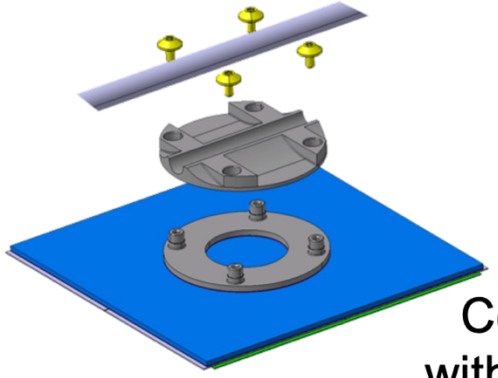
Module Cells

(Module + PG tile + Cooling Block)

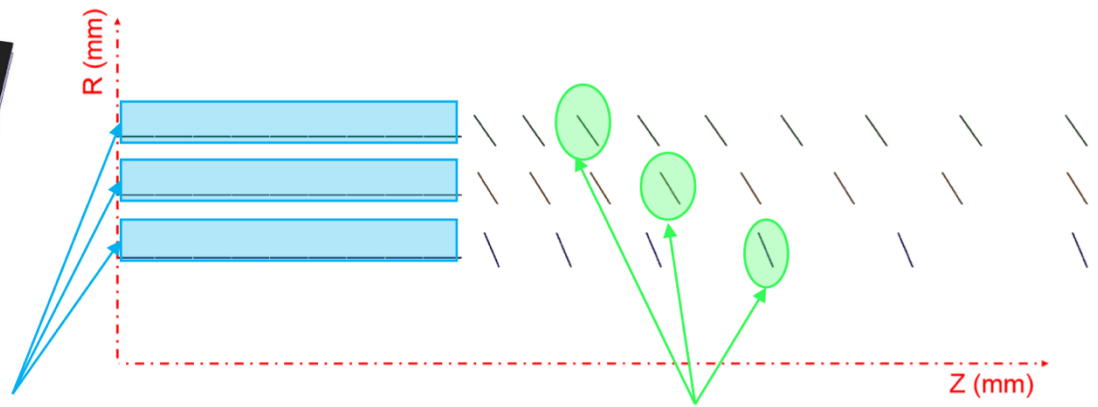




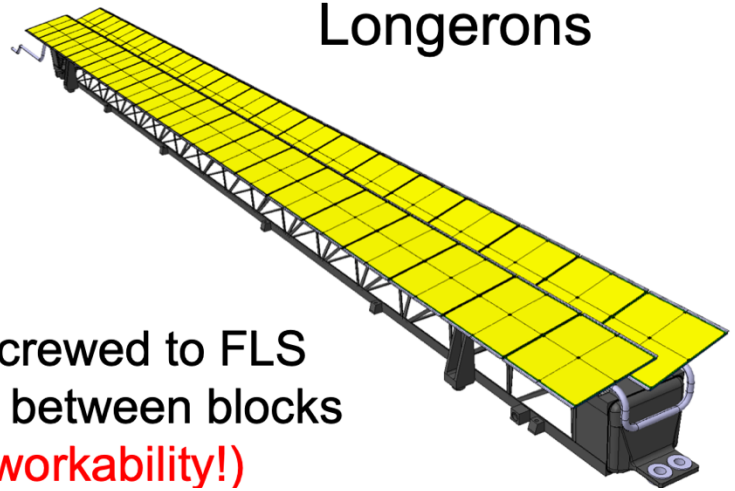
Cells screwed to FLS with TIM between blocks (re-workability!)

Functional Local Supports

(Base Blocks + Cooling Pipe + CFRP Support Structure)



Longerons



Inclined Half-Rings

Cell Loading

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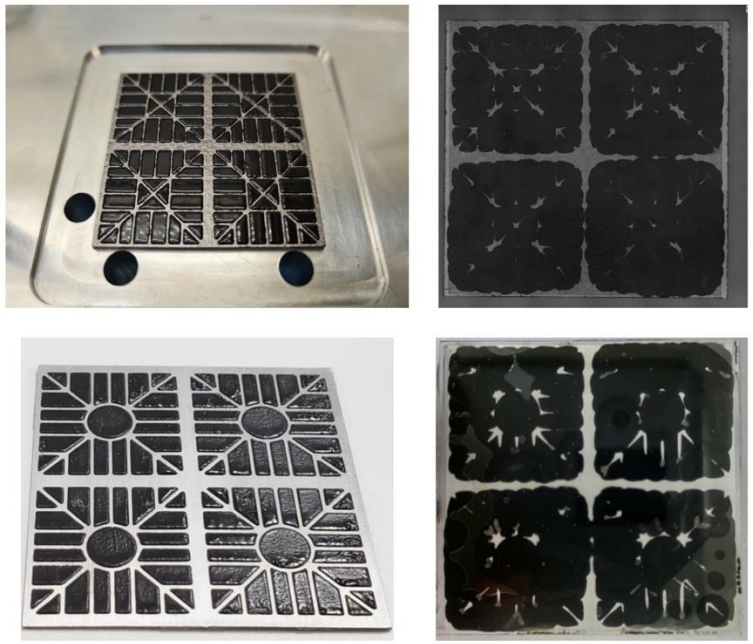
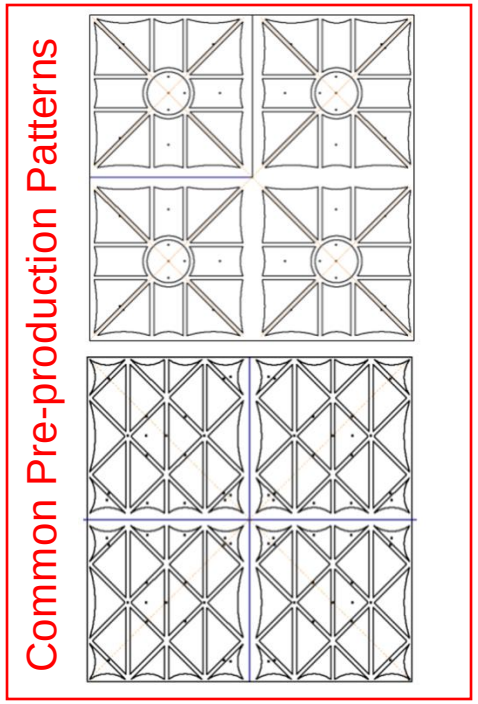
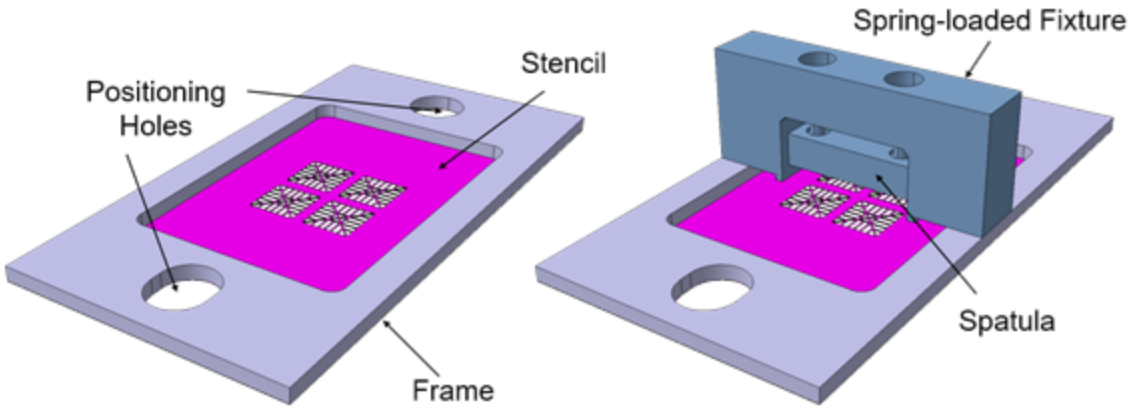
- Stainless-steel stencil with water-jet/laser cut pattern (150µm-thick)
- Fast, simple and reliable (developed @ UniGe & Japan for loading Methods I & III)
- Pattern combines circular/triangular/rectangular glue areas with scape paths for air trapped below each FE chip → Curved edges added for preproduction







Loaded Cell Metrology

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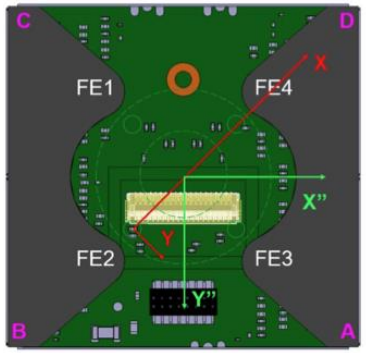
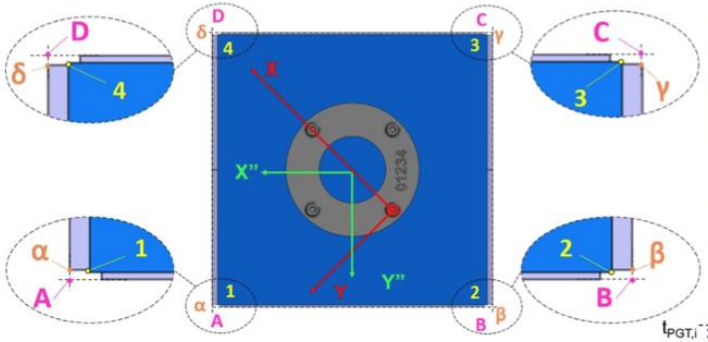
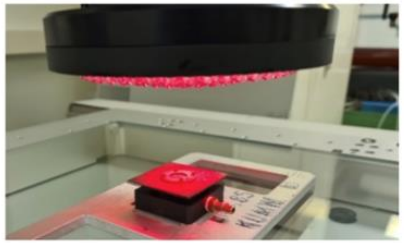
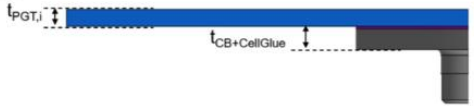
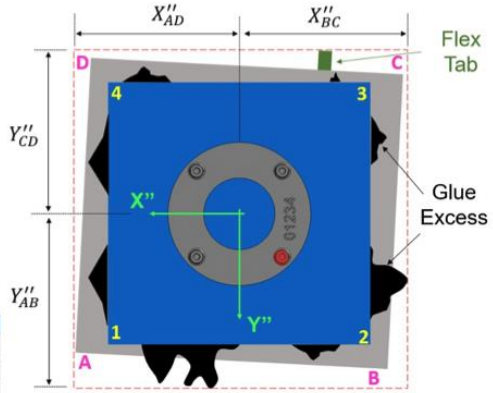
- Optical metrology survey of the backside of the loaded Module Cell
  1. Loading accuracy
  2. Envelope control
  3. Estimated glue thickness











Results of Metrology Survey of Module Cell					
Module Corner	FE Chip	Measured Coordinates of the Module Corners		Measured Coordinate of FE Chip Corners	Estimated Glue Thickness at Module Corners
		X''	Y''	Z''	$t_{STYCAST}$
A	FE3	X_A''	Y_A''	Z_α''	$\lvert Z_\alpha''\rvert - t_{CB+CellGlue+PGT,1}$
B	FE2	X_B''	Y_B''	Z_β''	$\lvert Z_\beta''\rvert - t_{CB+CellGlue+PGT,2}$
C	FE1	X_C''	Y_C''	Z_γ''	$\lvert Z_\gamma''\rvert - t_{CB+CellGlue+PGT,3}$
D	FE4	X_D''	Y_D''	Z_δ''	$\lvert Z_\delta''\rvert - t_{CB+CellGlue+PGT,4}$

Metrology results stored in ITk PDB

- Assess compatibility with longeron integration
  (Position in Y''-axis critical: Y_A'', Y_B'', Y_C'', Y_D'', Y_{CD}'', Y_{CD}'')
- Identify fluctuations across sites/operators

20UPGM22601098

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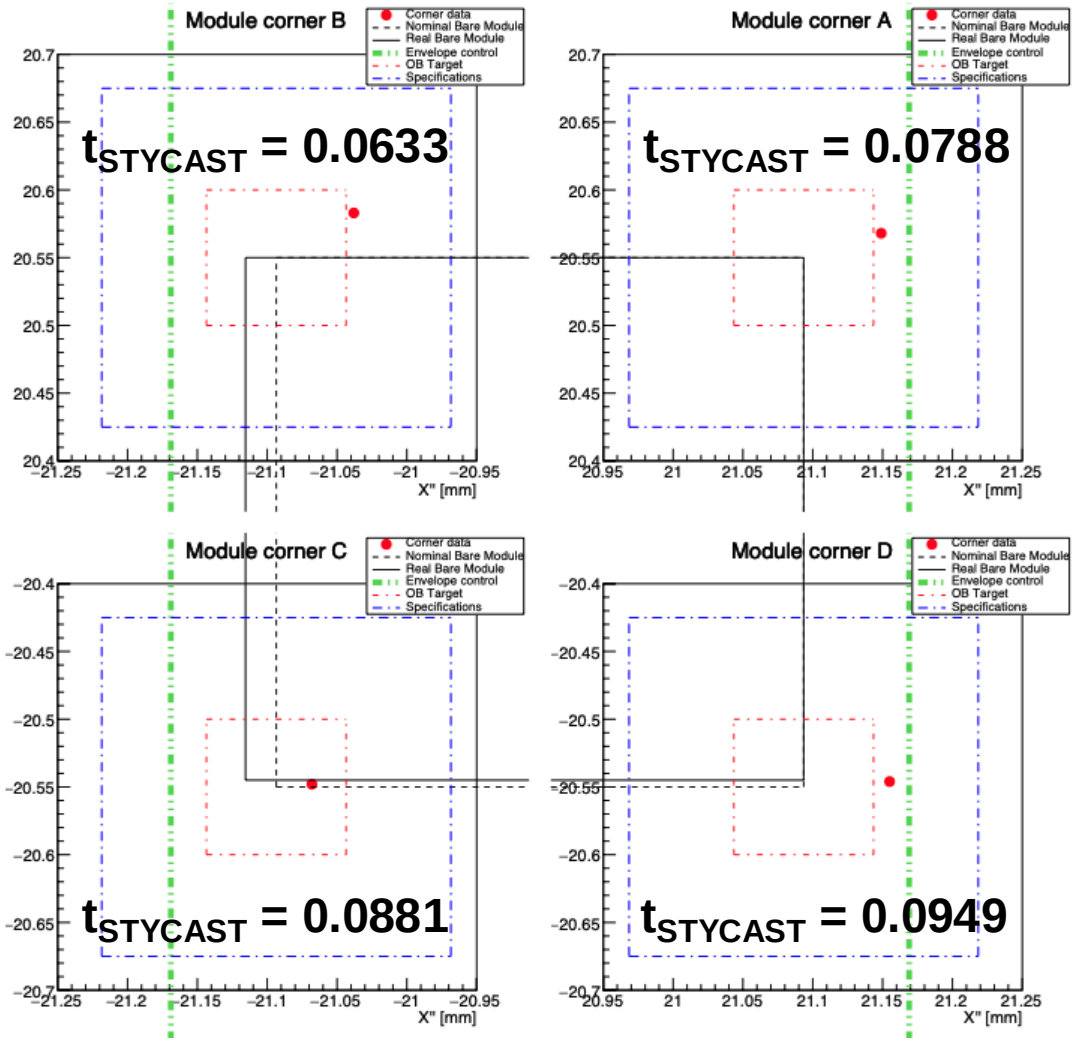

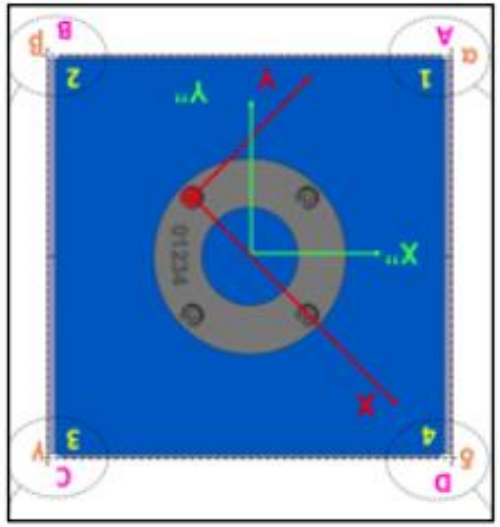

Red dots: measured corners
Black dotted line: bare module design size
Red dotted line: OB target (±50 μm)
Blue dotted line: Specifications (±125 μm)
Green dotted line: Envelope
Horizontal: X" axis
Vertical: Y" axis

- Module Thickness
  - A: 0.6998
  - B: 0.7003
  - C: 0.7091
  - D: 0.7089
- Cell Thickness
  - A: 0.621
  - B: 0.637
  - C: 0.621
  - D: 0.614

Loaded Cell QC

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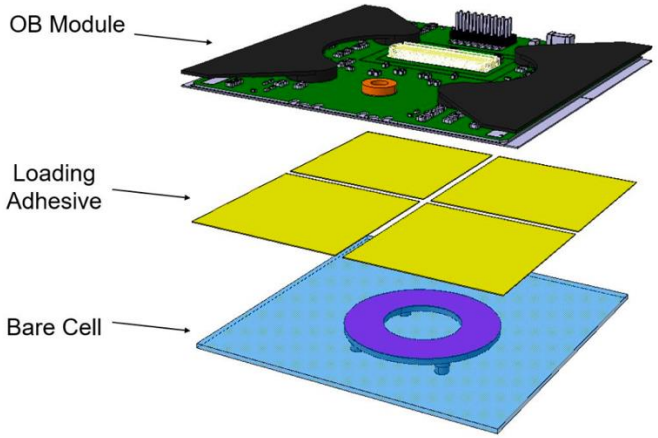
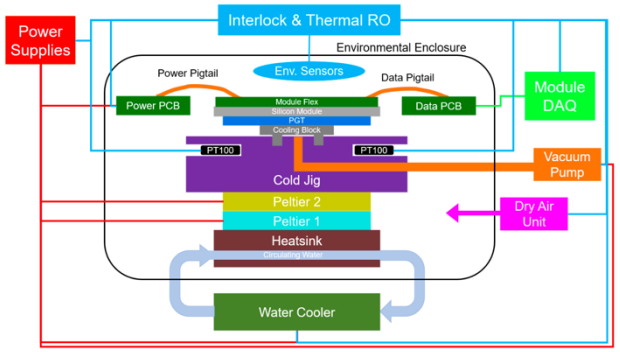
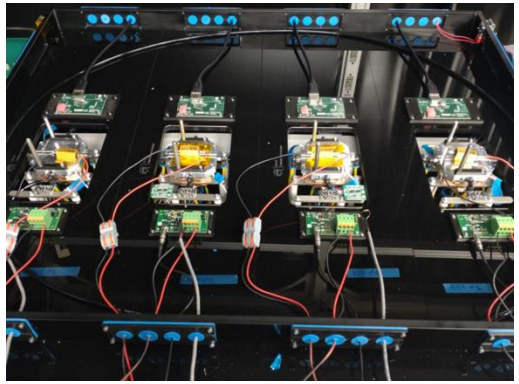
- OB “modules” will be shipped to cell loading site for cell loading
  - at cell loading stage, cooling cell will be attached to the module
  - the performance of the module including the thermal conductivity will be evaluated with common cell qc box
  - measure temperature sensors on the module
  - check correlation with power consumption of FEs







Thermal Measurement

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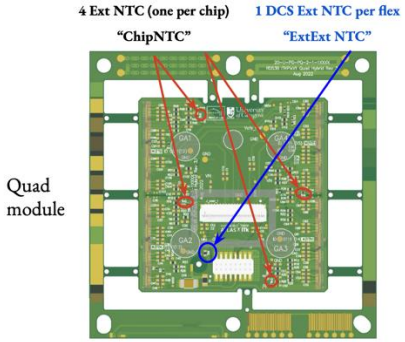
- To evaluate thermal conductivity, we would like to measure
  - temperature sensors on the module
    - 5 NTCs
    - 3 MOS sensors on each chip
  - cooling head temperature
  - applied voltage to FEs
- most of them can be readout via vmux
  - via vmux
    - 4 NTCs, MOS sensor, VDDA/D, VINA/D
    - already exist in AR and SLDO (VDDA/D, VINA/D)
  - via influxdb (will not be implemented directly)
    - ext. ext. NTC
    - cooling head temperature
    - module power at PSU(?) which can depend on each sites

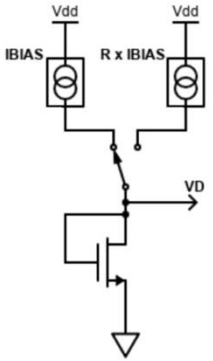
5 NTCs on the FPC



Vmux 2	NTC_PAD voltage
Imux 9	NTC_PAD current

$$T = 1/(A + B\ln R + C(\ln R)^3)$$

3 Temp Sens on in the chip



Vmux14	TEMPSENS Ana. SLDO
Vmux16	TEMPSENS Dig. SLDO
Vmux18	TEMPSENS center

$$T = \Delta V_D \times \frac{q}{N_f \times k_B \times ln(R)}$$

Results @ KEK

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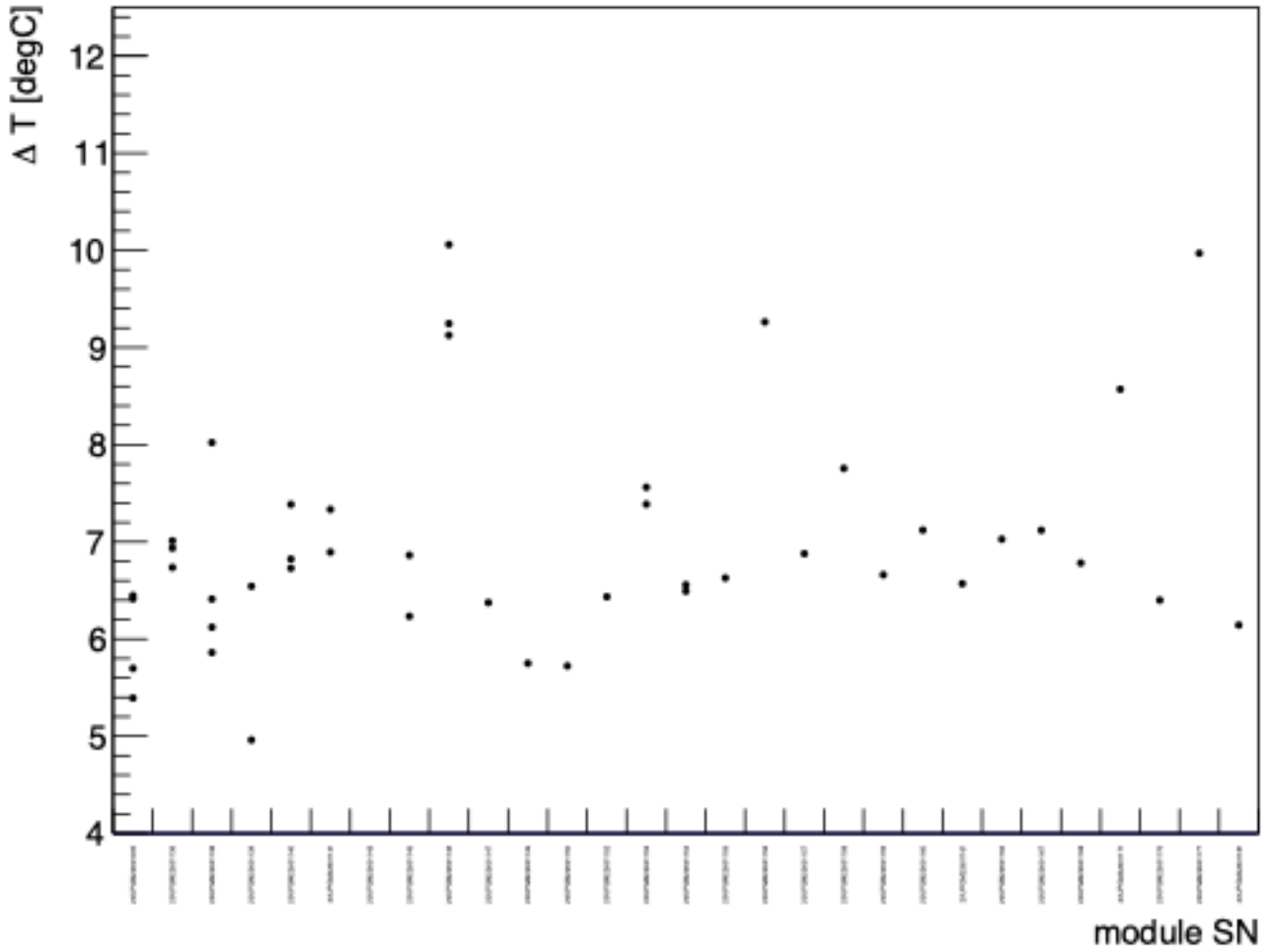
- ΔT ($T_{\text{module NTC}}$ - $T_{\text{cooling head}}$)
  - testing at warm (20 degC)
    - showing only
  - for chip1
  - almost all chips distributed around 6 - 7 degC
  - repeatability: at most $\pm$1 degC



First Integration!!

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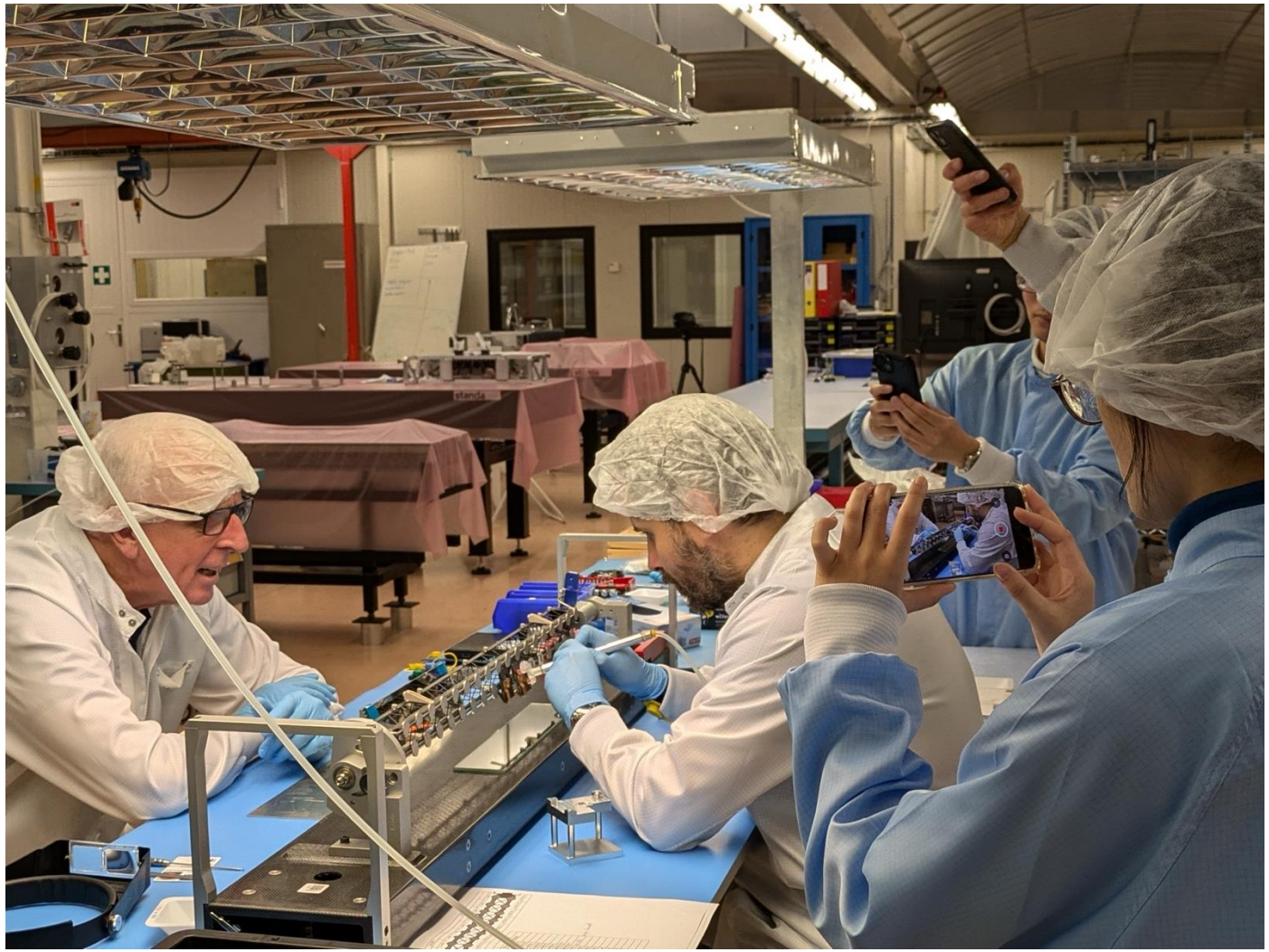

Summary

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- KU keep contributing to the ATLAS ID (SCT) Operation
- HL-LHC
  - for further physics research
- ITk Upgrade
  - 140 prototype modules have been produced as pre-production
    - many updates for the system has been done and scheduled
  - Mass production have been started
  - KU contributed to module assembling / cell loading, module production and testing

Backup

Results @ KEK

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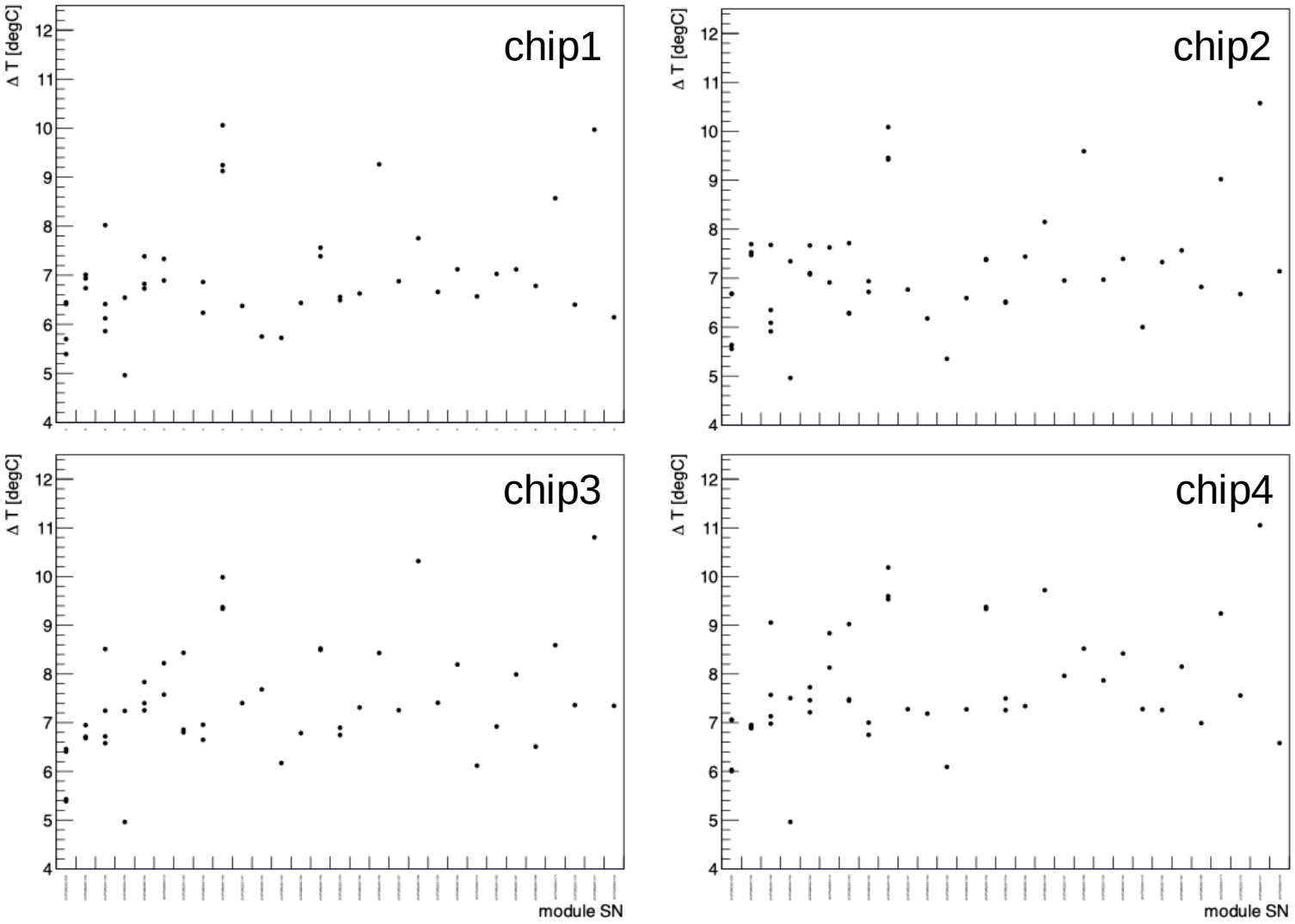

- ΔT ($T_{\text{module NTC}}$ - $T_{\text{cooling head}}$)
  - testing at warm (20 degC)
    - showing only set temp $\pm$1 for ext. NTC
  - chip4 shows higher than others
  - distributed around 7 degC
  - repeatability: at most $\pm$1 degC

Results @ KEK

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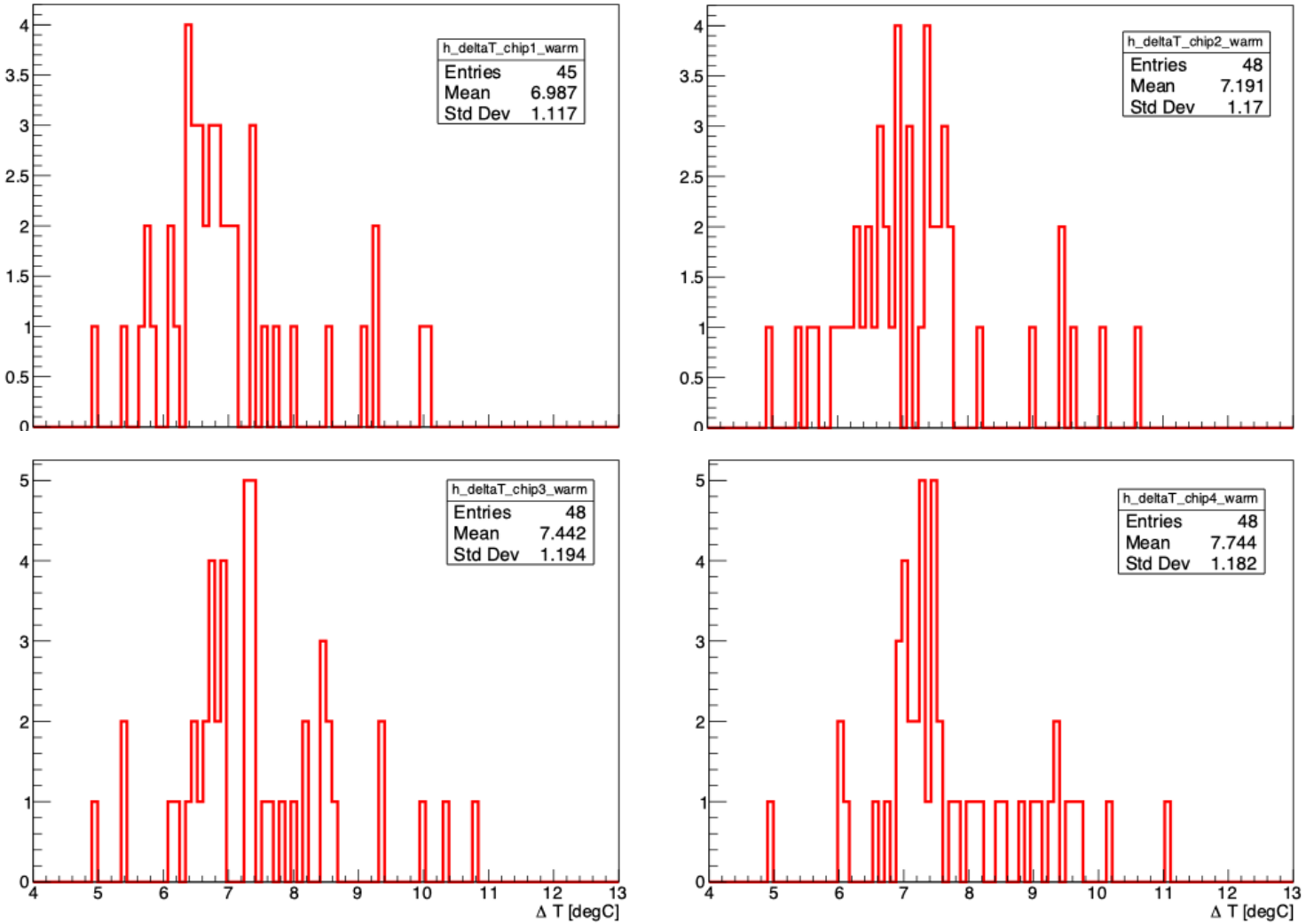

ΔT ($T_{\text{module NTC}}$ - $T_{\text{cooling head}}$)

- testing at warm (20 degC)
  - showing only set temp $\pm$ 1 for ext. NTC
- chip4 shows higher than others
- distributed around 7 degC and there are several module with higher ΔT

Results @ KEK

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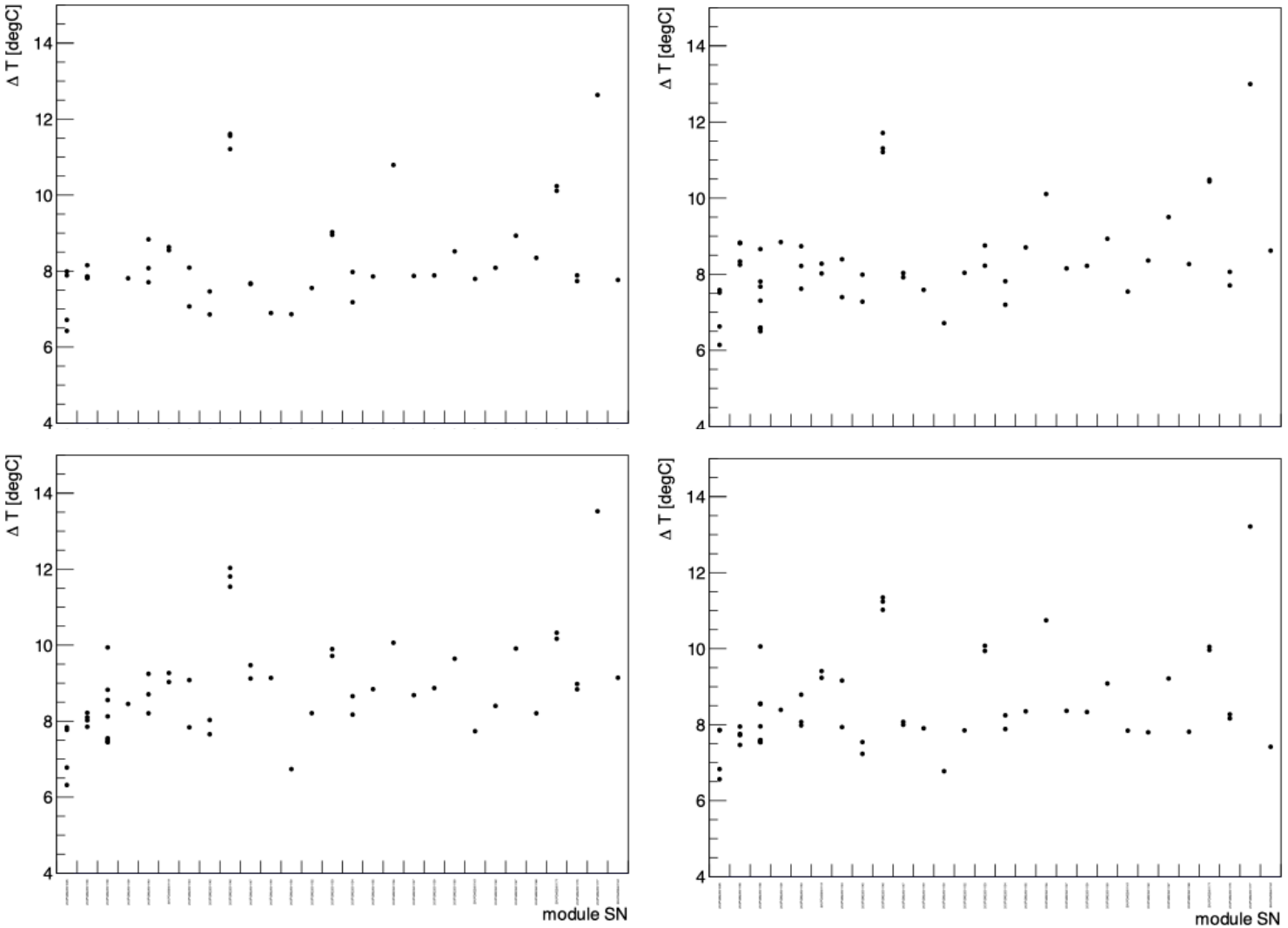

ΔT ($T_{\text{module NTC}}$ - $T_{\text{cooling head}}$)

- testing at cold (-15 degC)
  - showing only set temp $\pm$5 for ext. NTC
- every chip shows similar distributions
- distributed around 8 degC
- repeatability: at most $\pm$1 degC

Results @ KEK

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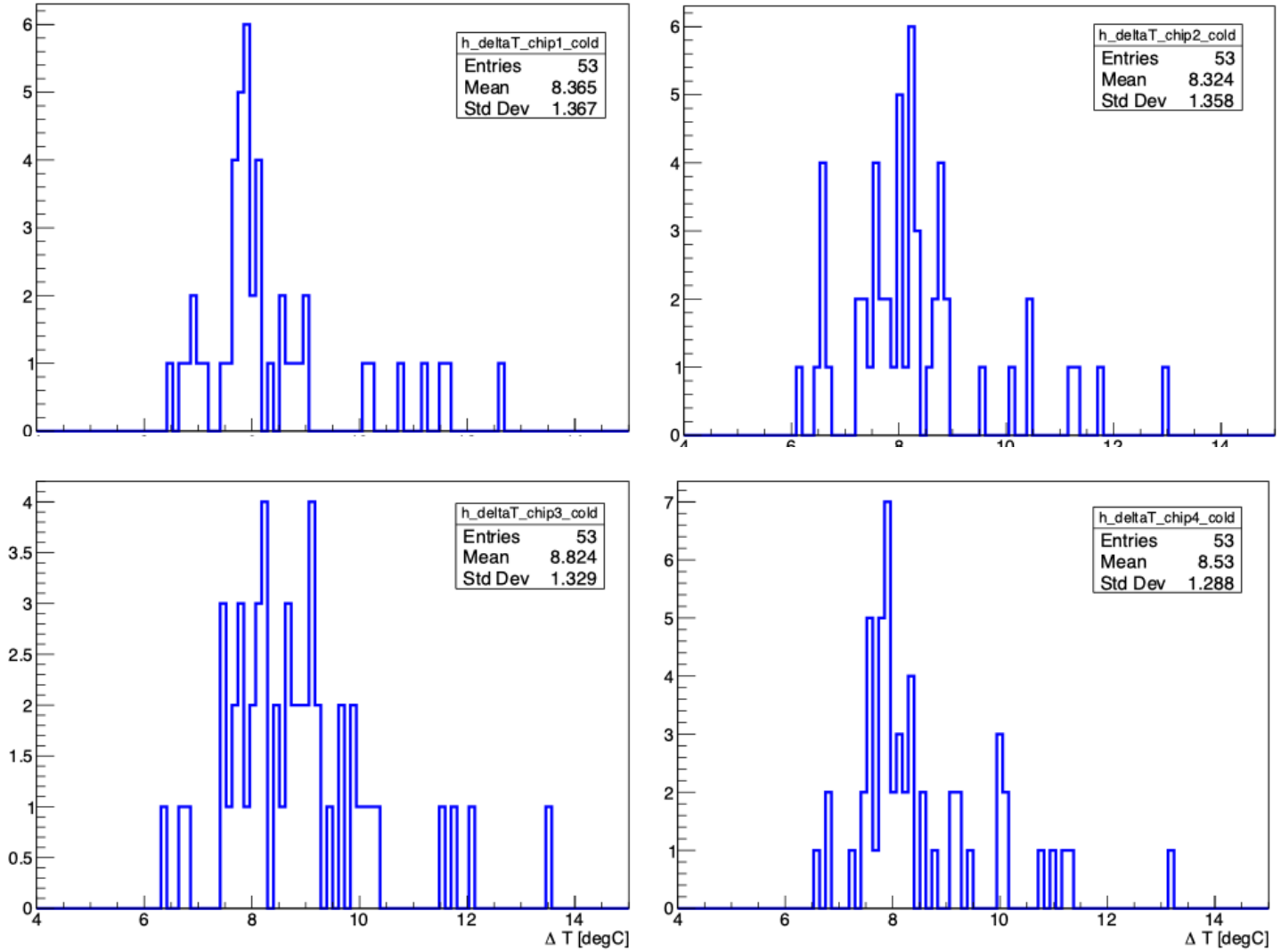

- ΔT ($T_{\text{module NTC}}$ - $T_{\text{cooling head}}$)
  - testing at cold (-15 degC)
    - showing only set temp $\pm$5 for ext. NTC
  - distributed around 8 degC
  - every chip shows similar distributions

Results @ KEK

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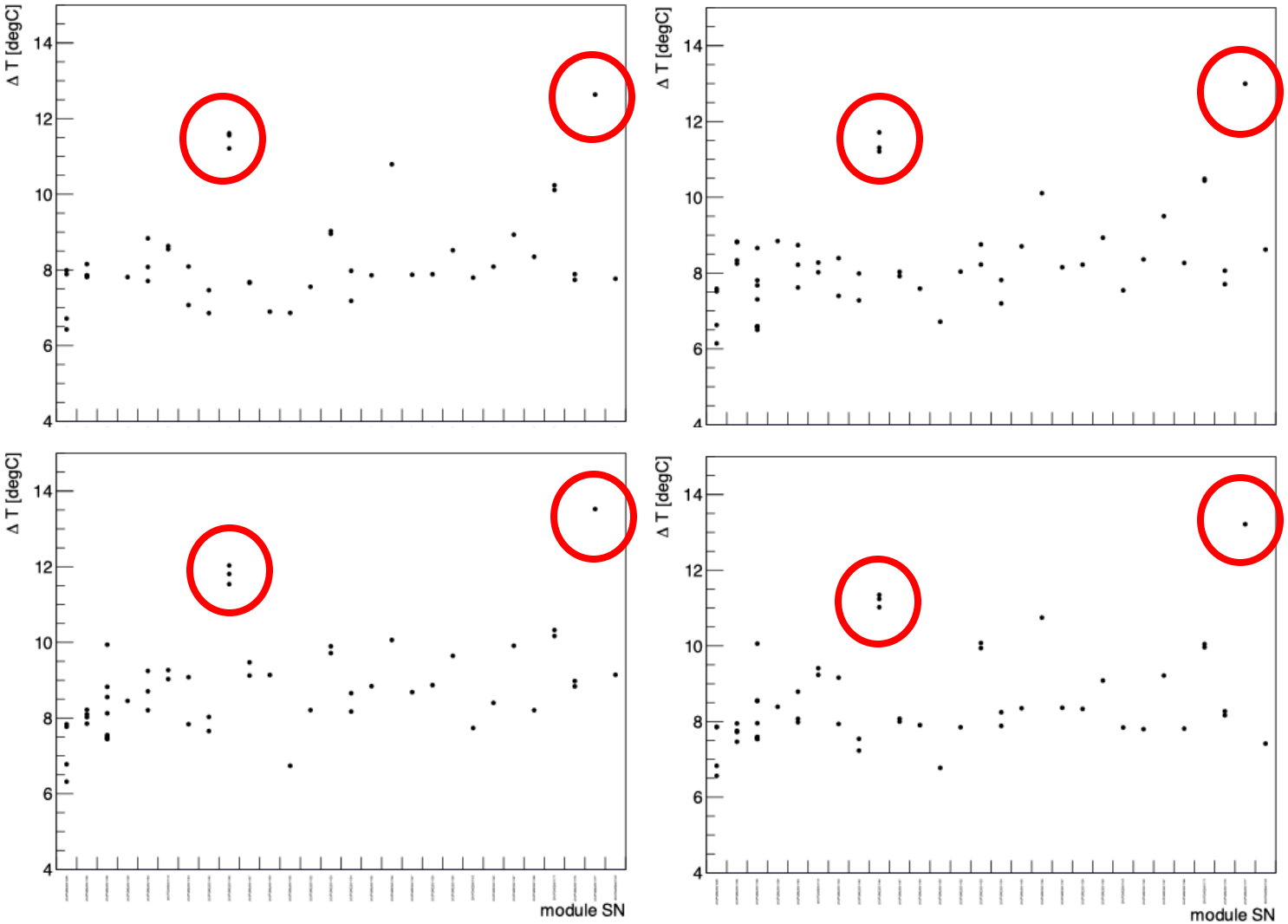

There are two relatively worse thermal conductivity modules

- The cell of them looks different from others

“normal” cell

“bad” cell

Comparison of tests @ CERN

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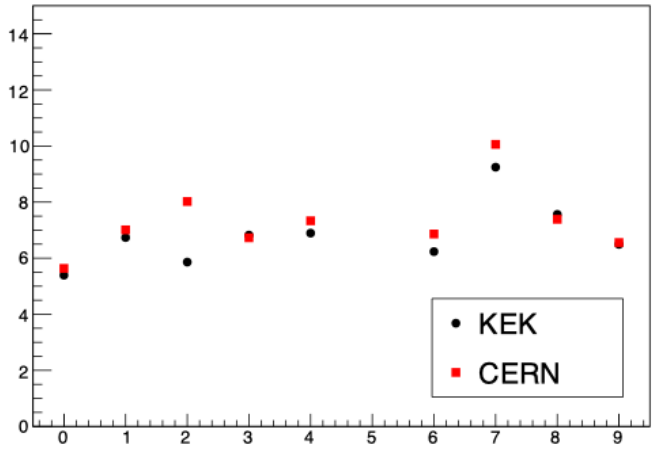

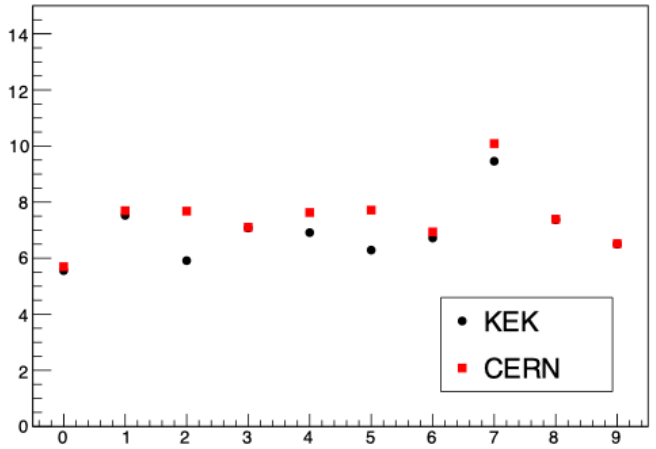

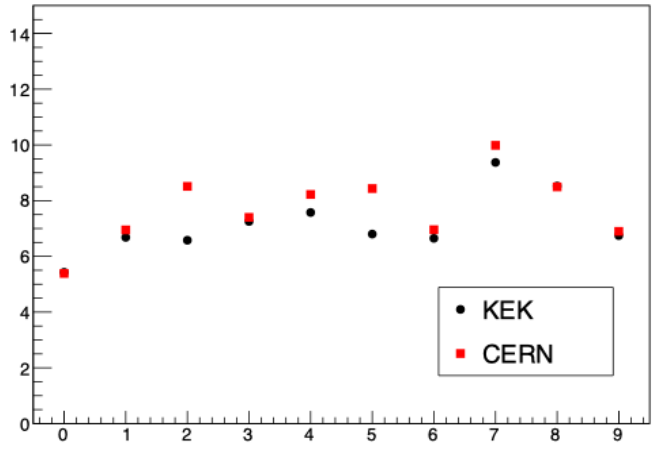

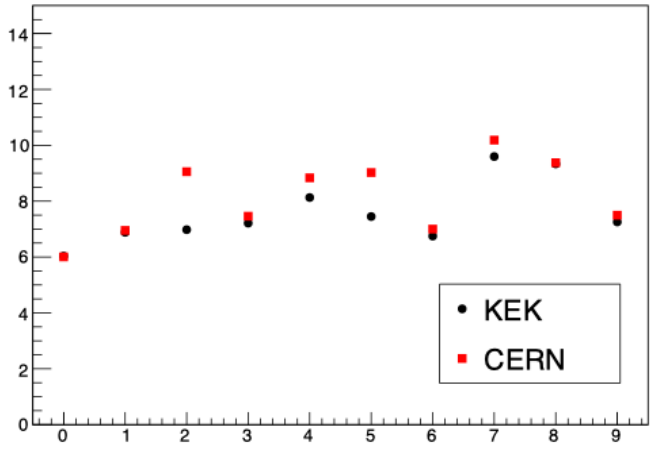

Loaded Cell Metrology 3

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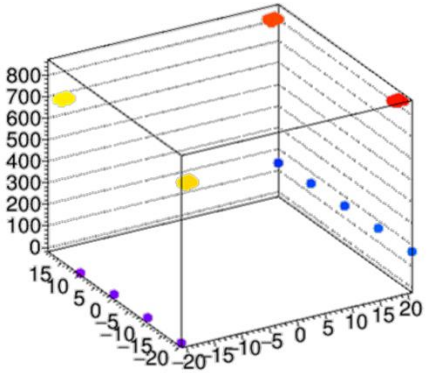
- Optical metrology survey of the backside of the loaded Module Cell
  1. Loading accuracy
  2. Envelope control
  3. Estimated glue thickness

KEYENCE VR-6000

1mm x 1mm

- Measured by two steps
  1. Cell measurement at KEK
     - will be included in KEK Fuji shift
     - need to consider how to handle data
  2. Loaded cell measurement at REPIC
     - will be included in REPIC shift
     - already implemented, in terms of the measurement
     - localDB



4x4 with 500um pitch